

GENERATING PWM WAVEFORMS USING THE IXDP610A

Abstract

The IXDP610 is a digital pulse width modulator that is targeted for microcontroller and microprocessor based systems used for switching power bridge applications, PWM controlled current or voltage sources, and other switching based designs. The IXDP610 excels in switch mode applications that require precise digital control of the PWM waveform parameters of PWM cycle time, duty cycle, duty cycle resolution and dead time interval.

Contact: support@ixysrf.com
<http://www.ixysrf.com>

INTRODUCTION:

The IXDP610 Digital Pulse Width Modulator (DPWM) is a programmable CMOS device which accepts digital pulse width data from a microcontroller or microprocessor and generates two non-overlapping, pulse width modulated signals for direct digital control of switching power bridges or switch mode based power supplies. To achieve success in designing with the IXDP610 the basic concepts surrounding pulse width modulated signals must be understood. From these concepts the proper hardware design can be implemented and then the IXDP610 configuration can be specified.

DISCUSSION:

The IXDP610 is designed to generate complementary square wave output waveforms for pulse width modulation (PWM) applications. To understand how to configure the IXDP610 to obtain the desired PWM waveform some basic concepts need to be explored. This application note will explain the concepts of PWM cycle time, pulse 'ON' time (also called duty cycle) duty cycle resolution and programmable dead time. From a basic understanding of these concepts the designer will be able to define the proper configuration for the IXDP610 for their PWM application.

When designing a PWM waveform one of the first parameters to define is the PWM cycle time. The PWM cycle time is the interval between successive pulses. It is the inverse of the PWM frequency. For applications using the IXDP610 this parameter is important since it is dependent upon the input clock frequency. The PWM cycle time should be the main consideration when selecting the external clock frequency.

The IXDP610 is capable of operating in 7-bit or 8-bit resolution. In 7-bit resolution the PWM cycle time is 128 counts of the input clock. In 8-bit resolution the PWM cycle time is 256 counts of the input clock. This leads to the following relationships. (See Figure 1 for a graphical representation of the PWM cycle time.)

$$T_{cycle} = \frac{T_{clk}}{2^N} \text{ where } N = 7 \text{ or } 8 \text{ bit resolution}$$

and

$$F_{cycle} = \frac{F_{clk}}{2^N} \text{ where } N = 7 \text{ or } 8 \text{ bit resolution}$$

where:

$$F_{cycle} = \frac{1}{T_{cycle}}$$

$$F_{clk} = \frac{1}{T_{clk}}$$

The final variable within the IXDP610 has to modify the PWM cycle time is the DIV bit in the IXDP610 control register. It is bit 5 in the control register and it enables a divide by two of the input clock. Here is the revised PWM cycle equation factoring in the effect of the DIV bit being set.

$$T_{cycle} = \frac{2 * T_{clk}}{2^N} \text{ where } N = 7 \text{ or } 8 \text{ bit resolution}$$

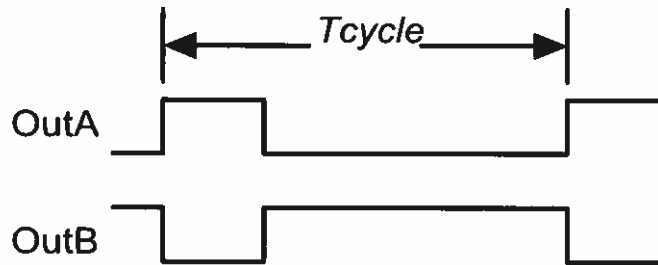


Figure 1: PWM Cycle Time with No Dead Time Intervals

Once the PWM cycle time is defined it is necessary to specify the PWM pulse width register to set the 'ON' time. This parameter, also called the duty cycle, defines when the non-inverted output is logic high, or 'ON'. Conversely, it defines when the inverting output is logic low or 'OFF'. It is configurable from a value of 0 to 2^N where $N = 7$ or 8-bit resolution. When the pulse width register is programmed with a 0 or a 1 the non inverting output will be a DC logic low and the inverting output will be a DC logic high. When programmed with $2^N - 1$ where $N = 7$ or 8-bit resolution the non-inverting output will be a DC logic high and the inverting output will be a DC logic low. These two states can be used for braking or DC operation depending upon the user specific hardware after the IXDP610. When the pulse width register is programmed with any value from 2 to $2^N - 2$, a switching wave from with a duty cycle that follows this relationship will result.

$$Duty_Cycle = \frac{PW}{2^N}$$

where

$N = 7$ or 8 bit resolution and PW is any count value from 2 to $2^N - 1$

(See Figure 2 and Table 1 for additional representations of the PWM duty cycle)

Pulse Width Count (Binary)		Resulting Duty Cycle (%)
7-Bit Resolution	8-Bit Resolution	
0000 0000	0000 0000	0.0
0000 0001	0000 0001	0.0
--	0000 0010	0.78125
--	0000 0011	1.171875
0000 0010	0000 0100	1.5625
--	0000 0101	1.953125
0000 0011	0000 0110	2.34375
--	0000 0111	2.734375
0000 0100	0000 1000	3.125
.	.	.
.	.	.
.	.	.
0100 0000	1000 0000	50.0
.	.	.
.	.	.
.	.	.
0111 1101	1111 1010	97.65625
--	1111 1011	98.046875
0111 1110	1111 1100	98.4375
--	1111 1101	98.828125
--	1111 1110	99.21875
0111 1111	1111 1111	100.0
1XXX XXX	--	100.0

Table 1: PWM Duty Cycle as a Function of Pulse Width Count

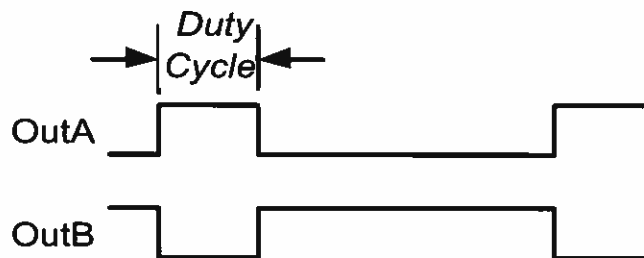


Figure 2: PWM Duty Cycle with No Dead Time Intervals

From Table 1 the concept of duty cycle resolution or pulse 'ON' resolution can be understood. The duty cycle resolution is the minimum discrete step the IXDP610 can make between possible duty cycles. In 7-bit resolution the minimum step is 1.5625%. In 8-bit resolution the minimum step is half of that or 0.78125%. This is the discrete accuracy of an IXDP610 implementation. It will correlate to the minimum control step size of the device being controlled. (i.e. speed of a motor, volts or amps of a switching source, etc..)

The final parameter that defines the IXDP610 PWM output waveform is the dead time. Since transistors do not have instantaneous turn off there is potential for a short circuit current to pass between the two transistors used in a half bridge configuration. To prevent this condition the IXDP610 has the ability to create two non-overlapping signals. The dead time is the time between the two outputs asserting logic high. In a PWM waveform with no dead time allotted, when the non-inverting output goes low the inverting output transitions high at the same time. (And the inverse is true, when the inverting output goes low and the non-inverting output goes high at the same time.)

The dead time count can be set from 000b to 111b. This allows for 8 possible dead times, each bit in this count represents two clock cycles, therefore the dead time can be set from 0 to 14 clock periods. In typical PWM cycles that are switching, there are two dead times as illustrated in Figure 3. The first is when the non-inverting output goes from low to high. This is concurrent with the inverting output transitioning from high to low. During this dead time period the non-inverting signal is delayed by the dead time count, and the ON time is shortened by the dead time. The second dead time occurs when the inverting output transitions from high to low and the non-inverting signal transitions from low to high. Again the signal going high is shortened by the dead time.

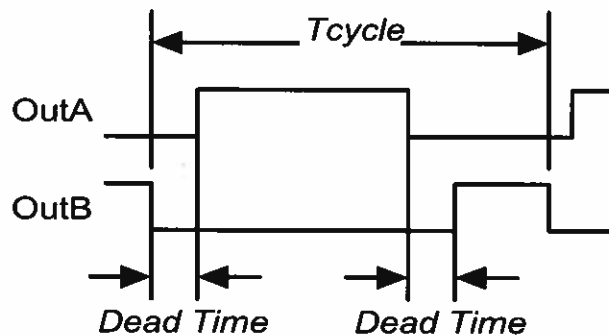


Figure 3: PWM Waveform with Dead Time Intervals

CONCLUSION:

The concepts of PWM cycle time, dead time, duty cycle, and duty cycle resolution create the IXDP610 output waveform. Understanding their interdependence is the key to creating a successful hardware design and software configuration when using the IXDP610. When designing with the IXDP610 the most critical hardware design choice involves the external clock frequency. The external clock directly defines the PWM cycle time, duty cycle resolution and dead time intervals. The configurable nature of the IXDP610 duty cycle allows the end user the opportunity for precision control, low power states, brake states, and DC operation. The additional feature of dead time control improves efficiency by eliminating potential short circuit currents in the power transistors used in switch mode architectures. With all of these options in one device the IXDP610 is an essential tool for any design that requires the precision of digital control with power electronics used in switching architectures.