1X6610 Signal/Power Management IC for Integrated Driver Module

Application Note
IXAN007501-1215

Introduction

This application note describes the IX6610 device, a signal/power management IC creating a link between a microcontroller unit (MCU) and isolated high speed IGBT/MOSFET gate drivers IX6611.

The IX6610 IC contains the circuit blocks required to operate a bidirectional interface between the MCU and drivers. This device provides the power required to drive the isolated gate drivers and MCU from a single +15 V power source while maintaining high voltage isolation between the MCU and gate drivers.

The IX6610 device also implements monitoring and protection functionality such as a +15 V supply undervoltage/overvoltage lockout and thermal shutdown. It is designed to operate within a temperature range of –40°C to +85°C, and is available in a 28-lead TSSOP package with an exposed pad.

Features

The IX6610 device offers the following features:

- Transistor–Transistor Logic (TTL) level microcontroller interface
- Signal inputs/outputs are compatible with the pulse transformer to enable communication with a galvanically isolated gate driver
- Inter-channel lock and dead time control
- Non-overlap operation of high side and low side drivers
- Up to 2 W output power to drive isolated gate drivers
- Up to 50 mA 3.3 V load capability output to drive the MCU
- Latched fault signals from gate drivers to allow the MCU to read fault information asynchronously
- Undervoltage and overvoltage lockout protection

General Description

The IX6610 device implements a dual channel bidirectional transformer interface to drive two secondary side intelligent IGBT drivers. This interface transmits the primary side input commands from the MCU to the secondary side, and the secondary side output and power supply faults to the MCU. Asynchronous data transmission is achieved through high-frequency narrow pulses to avoid duty cycle restrictions, achieve shorter delays, and prevent the occurrence of transformer core saturation issues. The IX6610 IC contains all of the necessary blocks to implement a power converter that supplies isolated power to the secondary side IGBT drivers. IX6610 is a primary side device with built-in interlock and dead time control that can be interfaced directly to a low voltage microcontroller and provides input signal conditioning and fault management.

Interface

TTL level compatible input signals INA and INB stemming from an external MCU are used to operate the secondary side IGBT/MOSFET drivers. These input signals are fed through the Schmitt trigger buffers to improve noise immunity. An input signal interlock function is implemented to prevent the simultaneous conduction of the secondary side IGBTs/MOSFETs, with priority designated to the INA signal. If the INA signal is active (logic one), the INB signal is ignored irrespective of its logic state until the INA signal becomes logic zero and the dead time set by the dead time capacitor CA expires.

A narrow pulse detector is implemented in the IX6610 device to prevent transmission of very narrow false PWM input signals to the IGBT drivers due to noise coupling at the input pins. Input signal pulse widths narrower than 100 ns are suppressed and pulse widths greater than 350 ns are transferred to the IGBT drivers.

In the half bridge driver configuration, dead time should be added to the incoming input signals to prevent shoot-through due to overlap of the high side and low side drivers. The required dead time should be programmed by the external MCU. The IX6610 IC also contains a dead time circuit that adds dead time to input signals INA and INB following the input signal interlock function. This dead time is used as a precaution only, in case of a software failure and applies if the dead time programmed by the MCU is shorter than the dead time set by the external capacitors at the CA and CB terminals.

To avoid the limitation of a transmitted maximum pulse width, the IX6610 device only transmits short pulses representing rising/falling edges of the INA (INB) signal at the TRAP (TRBP) and TRAN (TRBN) outputs respectively, while the IX6611 device restores the original INA (INB) pulse width on the secondary side; see Figure 1.

Figure 1. PWM Signal Transmission

Legend:

Channel 1 (blue) – input signal (INA/INB) from MCU
Channel 2 (magenta) – IX6610 TRAP/TRBP output
Channel 3 (green) – IX6610 TRAN/TRBN output
Channel 4 (red) – IGBT gate pulse at IX6611 output

Most standard telecommunication transformers can be used in this application. The use of pulse transformers with or without common chocks for Ethernet/10Base-T applications is recommended. Because the IX6610 TRAP (TRBP)/TRAN (TRBN) switches operate from a 3.3 V source, while the IX6611 input logic operates from a 5 V source, it is recommended to implement a 1:1.41 or 1:2 turns ratio in the transmit direction (from IX6610 to IX6611) and a 1:1 ratio in the receive direction (from IX6611 to IX6610) to improve noise immunity.

The IX6610 device has four single-ended receiver comparators which sense the presence of signals that are more positive than a fixed positive threshold value. A 1kΩ pull-down resistor to ground is connected to each of the receiver inputs. An external low pass filter can be implemented to prevent impulse noise from triggering the receivers. Receiver comparators are high speed Schmitt Trigger buffers with 1 V typical hysteresis. The secondary side power supply faults and IGBT power stage faults are transmitted back to the IX6610 IC (primary side) through a pulse transformer.

Table 1 lists the truth table for fault signals.

Table 1. Fault Signals Truth Table

Before FAULT RESET			After FAULT RESET			
FAULT1	FAULT2	Synchronized	FAULT1	FAULT2	SOURCE	SIGNAL
1	0	no	1	0	IX6610	Undervoltage
0	1	no	0	1	IX6610	Overvoltage
1	1	no	1	1	IX6610	Overtemperature
1	0	yes	0	0	IX6611	Undervoltage
0	1	yes	0	0	IX6611	Overvoltage
0	1	no	0	0	IX6611	Overcurrent

Fault signals generated by the IX6610 device are not synchronized with INA (INB) signals and cannot be reset via the MCU `FAULT RESET` signal. Fault signals remain active as long as the fault condition exists. However, when the fault condition disappears, the `FAULT` flag remains active till the MCU resets it.

Fault signals generated by the IX6611 device representing overvoltage and undervoltage conditions are synchronized with INA (INB) signals and are an echo of these signals. Such signals appear as fault outputs immediately following an attempt to transmit the INA (INB) signal when a fault condition on the secondary side exists. Fault flags representing these faults can be reset by the MCU, but will appear again at the next attempt to transmit an INA (INB) signal until the fault condition disappears. This allows the MCU to determine the source of the fault signals. The fault signal from the IX6611 device representing an overcurrent condition is not synchronized with the INA (INB) signal; however, the `FAULT` flag representing this condition can be reset by the MCU. It will be activated again if an overcurrent fault occurs at the next PWM cycle.

All fault conditions in the IX6610 device stop the execution of the PWM cycle. TRAN (TRBN) pulses are generated regardless of the position of the INA (INB) falling edge, effectively terminating the PWM cycle at both drivers.

All fault conditions in the IX6611 device stop the PWM cycle at the affected driver only. Therefore, it is up to the MCU programmer to determine the next step by identifying the cause of the fault. If fault conditions appear before the start of the PWM cycle, it will be ignored as long as fault conditions exist.

The typical interface connection between the IX6610 and IX6611 ICs is shown in Figure 2.

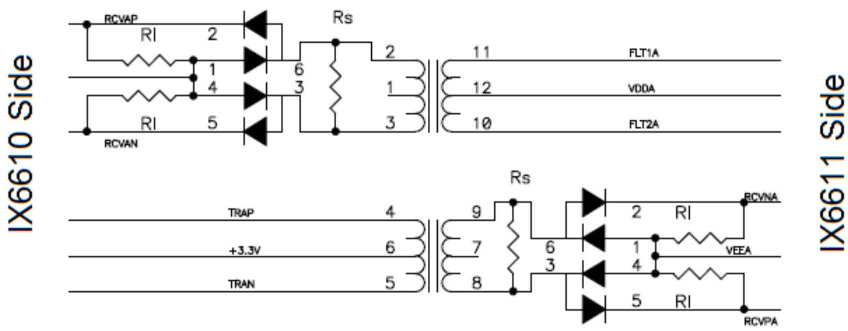

Figure 2. IX6610/IX6611 Signal Connection using an Isolation Transformer

Shunt resistor Rs is used to prevent a transformer's winding from ringing on the parasitic capacitance, which may create false triggering of the input of opposite polarity. Its value should be in the range of 20 Ω to 50 Ω. A diode matrix with low forward voltage forms a positive pulse only on load resistors Rl, from which the IX6610 and IX6611 devices read information. The recommended value of the Rl resistor is in the 50 Ω to 500 Ω range to maximize noise immunity. Decreasing the value of Rs and Rl resistors not only increases noise immunity but also increases the load on a transformer's primary side winding.

Power Block

The IX6610 power block is designed to provide up to 2 W of power to drive two isolated gate drivers (IX6611) and an MCU, if required, from a single +15 V supply.

The IX6610 IC utilizes push-pull converter topology, which allows multiple isolated outputs, step-up/step-down outputs, and/or inverted outputs with a low output ripple. The circuit drives two internal high current switches connected to an external center-tapped transformer providing dual isolated secondary side positive and negative voltages for the IGBT drivers and an isolated 5 V supply to the IX6610 device. The transformer's secondary to primary winding ratios determine the isolated output voltages.

The power converter has a start-up mode and a run mode. In the start-up mode, the converter operates from the internal oscillator and activates only a portion of the power switches to reduce the dynamic current consumption/power dissipation. After start-up, the converter activates all the power switches and goes into run mode. The power converter switches from start-up mode to run mode when the IX6610 device detects a reflected voltage threshold of 1.9375*V_{IN} on the TRDCP pin during the disabled driver period. The run mode is not initiated until the reflected voltage threshold detect has been valid for 128 clocks or ~1.28 ms. The transmit operation is also disabled during start-up mode to minimize current drawn on the secondary side. After run mode begins, the IX6610 IC no longer monitors the TRDCP voltage and continues in this mode of operation until a reset occurs, returning the power converter to start-up mode.

In run mode, the power converter operates either from an internal or external MCU clock, if it exists. An external clock may be used to minimize noise interference between the IX6610 devices used in multiphase applications such as motor drivers.

The push-pull block repeats the duty cycle of the external clock which allows for slight adjustments in secondary output voltage when an undervoltage or overvoltage condition occurs, by varying the duty cycle.

To prevent excessive power dissipation and potential failure of the IC due to a faulty clock, a watchdog timer is included. Whenever the push-pull converter clock period exceeds the watchdog timeout period (40 µs), the converter is disabled for the next 8 valid clocks.

The IX6611 device contains an internal LDO regulator with a 3.3 V output voltage to drive the MCU. The maximum load current at 50 mA for 100 ms enables easy MCU initialization. When the auxiliary winding voltage is less than 4.6 V, power to the LDO is provided by the 5 V start-up regulator of the IX6610 device. However, the auxiliary winding connected to the VAUX pin should be used to reduce power losses and to improve efficiency in run mode. A large ceramic bypass capacitor is required at the VAUX pin.

If an external 3.3 V source is used to drive the MCU, an internal LDO regulator should be disabled by applying logic level to the Mode pin to prevent competition between regulators. The Mode pin has an internal pull-down resistor and can be left open when the internal LDO is active.

A logic high level at the Reset pin disables the power converter and the LDO initiates the power converter start-up sequence, and resets the fault flags. Holding Reset low for sufficient time lowers the LDO voltage to a level at which a POR sequence in the MCU may be initiated. The Reset pin has an internal 20 KΩ pull down resistor.

A typical power transformer configuration is shown in Figure 3.

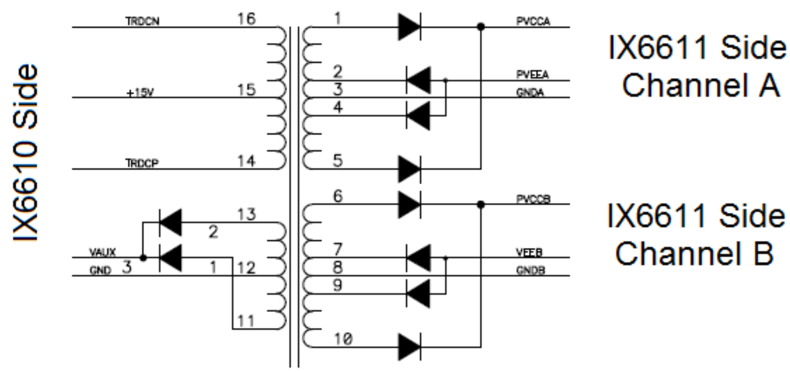

Figure 3.Typical Power Transformer Configuration for Half-bridge Applications

The IX6610 device contains a thermal shutdown circuit to protect the device against damage due to excessive die temperature. When the junction temperature exceeds 150°C, the power converter is disabled. The device resumes normal operation when the junction temperature falls below 130°C.

Layout Considerations

The IX6610 device is a high-frequency high current driver operating in very noisy environments such as high power motors, inductors, heaters, and other heavy industrial equipment. Close attention should be paid to the PCB layout to maximize noise immunity and the driver's performance.

Figure 4 depicts a recommended decoupling schematic and PCB layout for the IX6610 IC. The R1 Rbias resistor and C1 and C2 dead time setting capacitors should share a quiet signal ground (pin #2), which should be tied to power ground (pins #14 and #28) at one point only.

Close attention should be paid to minimum creepage distance between isolated parts of the design.

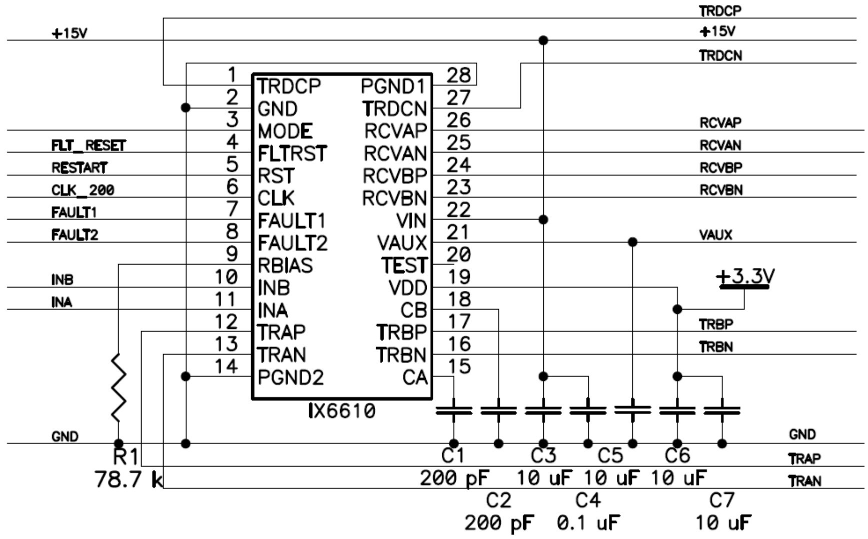

Figure 4. Recommended Decoupling for the IX6610 Device

A typical application schematic for a half-bridge configuration is shown in Figure 5 and the recommended layout is shown in Figure 6.

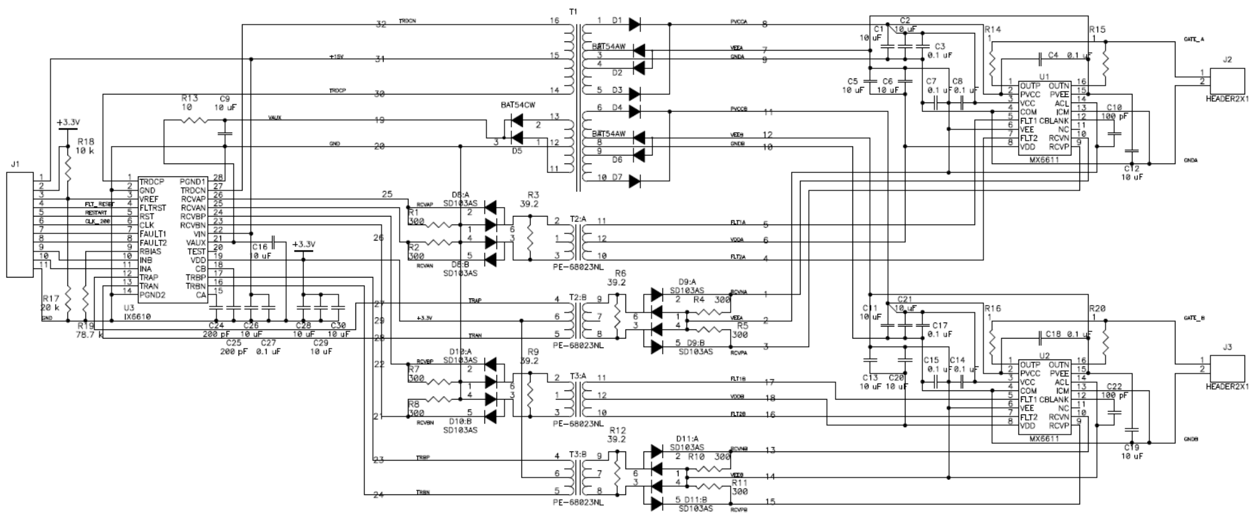

Figure 5. Typical Application Schematic for Isolated IGBT Driver in Half- bridge Configuration

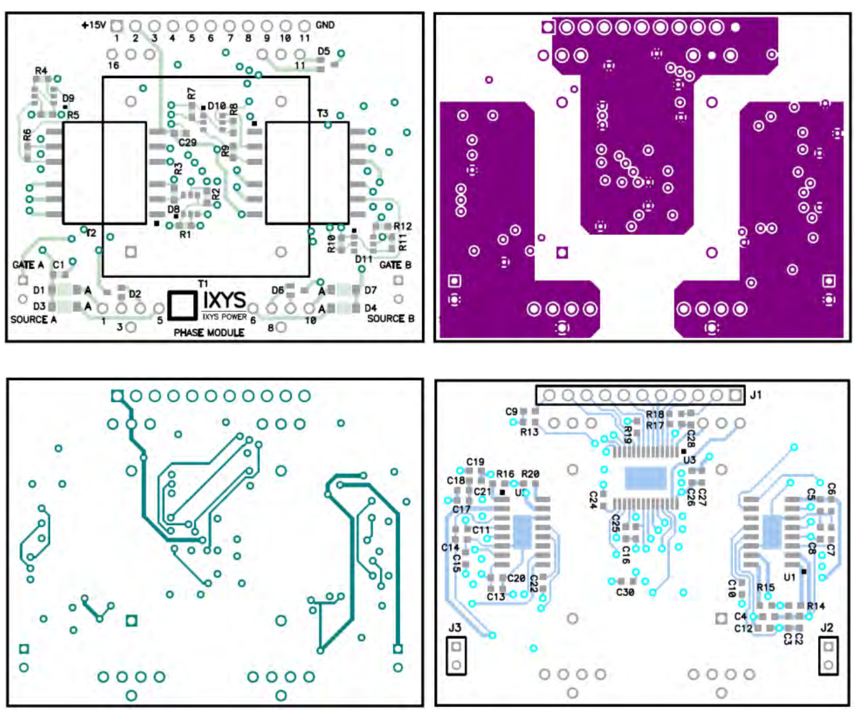

Figure 6. Typical Application Layout for an Isolated IGBT Driver in Half-bridge Configuration

(Top, Internal 1, Internal 2, and Bottom layers; Actual size)

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