Introduction

This application note describes the IX6611 device which is an intelligent high speed gate driver designed to drive IXYS IGBTs and power MOSFET devices. It also contains the circuit blocks necessary for pulse transformer isolated applications to galvanically isolate a signal source/recipient such as a microcontroller unit (MCU) from high power circuitry, maintaining bidirectional communication. This feature makes it possible to provide feedback signals to the MCU when fault conditions occur.

The IX6611 gate driver also implements monitoring and protection features such as undervoltage and overvoltage lockout (UVLO/OVLO), thermal shutdown, and external IGBT overcurrent and overvoltage protection. This device is designed to operate within a temperature range of –40°C to +125°C and is available in a 16-lead SOIC with an exposed pad.

Features

The IX6611 device offers the following features:

- Signal inputs/outputs are compatible with the pulse transformer to ensure communication with a galvanically isolated MCU
- 10 A peak source and sink current gate drive with separate source and sink outputs
- Negative gate drive capability to drive IGBTs
- Overcurrent protection with adjustable blanking time
- Advanced active clamping protection
- Undervoltage and overvoltage lockout protection
- Two 1 A pulse transformer drivers for fault signal communication

Gate Driver Description

The IX6611 device is designed to provide a gate drive for high power IGBTs by converting the incoming PWM logic signals into a +15 V/–5 V (with respect to COMMON) bi-polar gate drive signal with a typical 10 A peak drive current capability. Separate positive and negative gate driver outputs allow optimal IGBT turn on/off time without an external diode via a selection of serial gate resistors of different values (see Figure 1, R1 and R2 resistors). An internal dead time circuit eliminates the cross conduction of the source and sink outputs.

If the IX6611 gate driver is used to drive MOSFET devices and a negative offset for gate voltage is not required, VEE and PVEE inputs should be tied to COMMON. In this case, a negative voltage source is not used. Internal logic is powered from an internal V_{DD} source. The V_{CC} voltage should be at least 5 V above the UVLO threshold, as shown in the data sheet, to avoid detection of a UVLO condition.

The gate driver ensures IGBT overvoltage and overcurrent protection.

Active Clamping Protection

Active clamping protection feature prevents IGBT damage if the inductive load is turned off with a high inductive current. To avoid a situation in which the IGBT collector voltage easily exceeds breakdown limits and destroys the IGBT, consider keeping the IGBT in conduction mode until the energy stored in the inductor is insufficient to initiate a collector overvoltage condition. The IX6611 gate driver utilizes an ACL comparator with a 3 V threshold with respect to VEE voltage that may be used for implementing an advanced active clamping technique, as shown in the application circuit diagram in Figure 1.
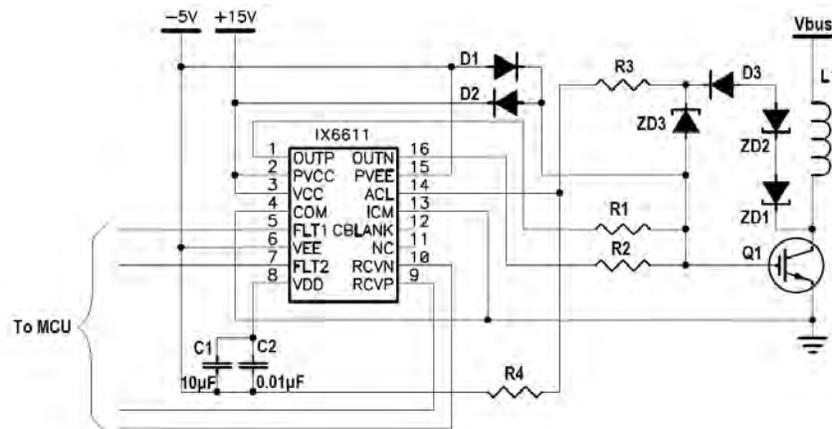
**Figure 1. Active Clamping using the IX6611 ACL Comparator**

The ACL comparator monitors voltage at the R3/R4 resistive divider, which is connected to the IGBT collector through the ZD1 and ZD2 clamp diodes. If the IGBT collector voltage exceeds a value equal to the $V_{ZD1} + V_{ZD2} + V_{ZD3} + V_{EE}$ threshold, current starts flowing into the OUTN gate driver output, creating a voltage drop across ZD3 and R2. A resistive divider should be chosen whereby the voltage drop across R4 exceeds the ACL comparator threshold of 3 V, i.e. $V_{ZD3}*R4/(R3+R4) > 3V$, assuming that the voltage drop across R2 is significantly less than V_{ZD3}.

Triggering the ACL comparator forces the gate driver output into a tri-state condition. The IGBT starts to turn on due to the breakdown diode current charging the IGBT gate. After the IGBT turns on, its collector voltage falls, the diode recovers from breakdown, and the ACL comparator turns on the OUTN output, which forces the IGBT gate low. This sequence may repeat several times until the energy in the external inductance is dissipated. The ACL comparator is active only when the driver's output OUTP is OFF.

The D1 and D2 diodes protect the IGBT gate from overvoltage if the voltage at the IGBT gate becomes more positive than V_{CC} or more negative than V_{EE}. The D3 diode protects the OUTP gate driver output from draining current into the collector when it becomes less positive than V_{CC}.

Overcurrent Protection

The IX6611 gate driver includes an Overcurrent Comparator (OC COMP) with a 300 mV threshold, which is used to sense IGBT overcurrent conditions. The IGBT emitter current sense can be implemented by using either a low value current sense resistor or an IGBT with a secondary current sense output. The current sense method works well for high gain IGBTs that do not have inherent short circuit protection; see Figure 2.
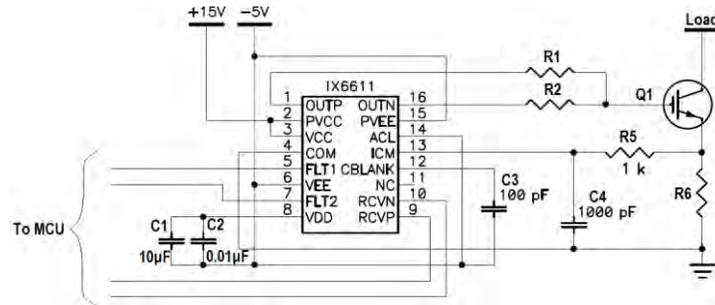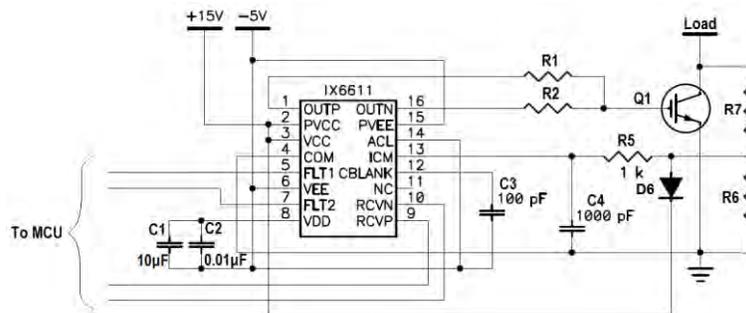

Figure 2. Overcurrent Protection using the IX6611 ICM Comparator and Current Sense Resistor

If an IGBT overcurrent fault occurs, the IGBT driver output is forced low for the remainder of the cycle. Normal operations resume at the beginning of the next PWM gate drive cycle. However, prematurely turning the IGBT off may cause an overvoltage condition at the IGBT collector. In this situation, the OUTP gate driver is turned off for the remainder of the cycle and the OUTN gate driver is controlled by the ACL comparator. Normal operations resume at the beginning of the next PWM gate drive cycle. A noise filter (R5C4) at the current sense input may be required due to low sense voltage.

An IGBT overcurrent fault event can occur any time during the ON time of the gate drive signal. When an overcurrent event occurs, the Output Fault Pulse Generator creates a narrow 200 ns pulse that is used by the fault control logic to communicate the fault condition to the MCU.

The OC comparator's input is grounded during the off time of the IGBT and remains grounded for a fixed amount of time immediately after the IGBT turns on, to prevent false tripping. The Leading Edge Blanking Circuit sets the blanking time, which is programmable by an external capacitor (see Figure 2, capacitor C3). A careful setup of the application board layout is mandatory due to low sense voltage.

Traditional desaturation protection can also be implemented using a large ratio resistive divider across the collector to the emitter, as shown in Figure 3.The R6/R7 resistive divider has two limitations regarding its value. A voltage drop across R6 should be above 300 mV to trigger the ICM comparator if an IGBT desaturation event occurs. Such a voltage drop should not exceed the V_{CC} voltage, when the IGBT is in an off state. If it is physically impossible, the clamping diode to V_{CC} should be used to prevent ICM comparator damage, as shown in D6, Figure 3.

Figure 3. Overcurrent Protection using the IX6611 ICM Comparator and IGBT Saturation Voltage

Undervoltage and Overvoltage Protection

The IX6611 gate driver contains undervoltage and overvoltage lockout comparators that monitor the positive power supply terminal. If, at the beginning of the PWM pulse positive power supply, voltage is below the UVLO threshold or above the OVLO threshold, the gate driver output is driven low and it skips that PWM pulse. However, if UVLO or OVLO conditions occur after the PWM pulse start, these conditions are ignored until the next PWM pulse.

If the positive power supply recovers from the fault condition, normal operations resume on the next PWM pulse. The UVLO circuit becomes operational at V_{CC} above 3 V and keeps the gate driver output low until V_{CC} rises above the UVLO threshold. Fault information is communicated to the MCU as narrow pulses. Based on the type of fault, the fault control logic selects narrow pulses either from the input interface or from the output fault pulse generator.

A UVLO fault condition is communicated to the MCU as an FLT1 pulse that is an input interface pulse representing the leading edge of the PWM pulse, delayed by the IX6611 gate driver's propagation delay time. An OVLO fault condition is communicated to the MCU as an FLT2 pulse that is an input interface pulse representing the trailing edge of the PWM pulse, also delayed by the IX6611 gate driver's propagation delay time. The IGBT overcurrent condition is communicated to the MCU as an FLT2 pulse from the internal output fault pulse generator, which is synchronized with the overcurrent event, but not with the leading/trailing edges of the input PWM signal. FLT1 and FLT2 outputs are built with open drain architecture and are capable of sinking up to 1 A current.

Interface

The IX6611 gate driver's input interface works in start/stop mode with a short positive pulse signal at the RCVP input. This represents the leading edge of the PWM pulse and a short positive pulse at the RCVN input represents the falling edge of the PWM pulse. The IX6611 device's pulse recovery logic reconstructs the PWM pulse and generates complementary signals at the OUTP/OUTN outputs.

Leading/trailing edge pulses can be as short as 100 ns. This allows the use of either a direct MCU connection with the driver or isolation transformers with small volt-second value to transmit PWM pulses with a duration ranging from 200 ns to infinity. Therefore, the IX6611 gate driver may be used not only for fast switching applications like motor drivers, DC/DC converters, or AC/DC PFC converters, but also for switches of high power devices operating once per day, and similar applications.

The RCVP/RCVN logic inputs threshold is more than 2.2 V for logic "one" and less than 1.0 V for logic "zero". To reject noise and high frequency interference, a well-matched full differential architecture is used at receivers with 1 V hysteresis Schmitt Trigger buffers. This architecture provides a direct connection of the MCU to the gate driver in case of the MOSFET as gate driver load with VEE/PVEE and COMMON pins tied together. Gate driver inputs are of high impedance; therefore, MCU outputs should be configured as low current outputs. MCU inputs receiving information about fault conditions should be configured as pull-up inputs.

If the IX6611 gate driver is used to drive an IGBT and a negative voltage source is required, logic signals should be transmitted and received with respect to negative V_{EE} sources that require MCU ground to be connected to negative voltage sources, which may not be convenient or possible. In such instances, an isolation transformer should be used to separate the MCU and driver. This allows for galvanic isolation of the MCU from the IX6611 gate driver and high power devices, thereby significantly increasing MCU noise immunity in high power applications.

The input interface to the gate driver is designed to be compatible with pulse transformers with small volt-second value, such as standard Ethernet/10Base-T isolation transformers PE-68023, PE-65745, PE-65454, or similar devices.

The recommended MCU/gate driver connection with an isolation transformer is shown in Figure 4.
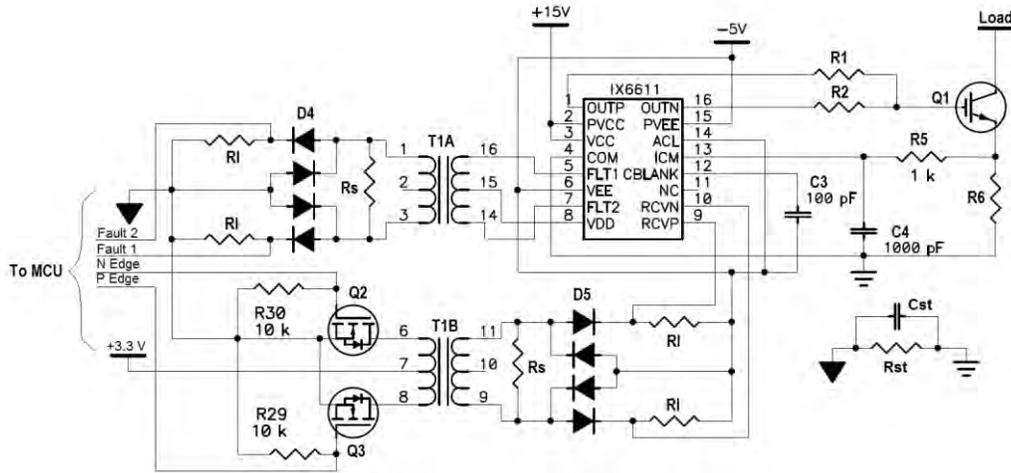
Figure 4. MCU Connection with the IX6611 Gate Driver using an Isolation Transformer

If MCU outputs are of low current capability, additional MOSFETs (Q2 and Q3) should be used to drive the transformer. It is recommended to use windings with a 1:1.41 or 1:2 ratio to improve noise immunity on the driver's secondary side, especially for low voltage MCUs (i.e. 3.3 V or less).

Pay attention to fault signals at MCU inputs, which should not exceed MCU limits, because the IX6611 drive transformer's winding from VDD is equal to a 5 V source, and voltage on the MCU side is equal to 5 V multiplied by the transformer's coefficient. If required, use only one half of the secondary winding to decrease twice the amplitude of fault signals applied to the MCU inputs. Additionally, the Rl resistors can be split to create a resistive divider for incoming fault signals.

Shunt resistor Rs is used to prevent the transformer's winding from ringing on parasitic capacitance, which may create false triggering of the input of opposite polarity. Its value should be in the range of 20 Ω to 50 Ω. The D4 and D5 diode matrix with low forward voltage form a positive pulse only on the Rl load resistors, from which the IX6611 gate driver and MCU read information. The recommended Rl resistors' value should be in the range of 50 Ω to 500 Ω to maximize noise immunity. Decreasing the value of Rs and Rl resistors not only increases noise immunity but also increases the load on the transformer's primary side winding.

To avoid static electricity accumulation, a high voltage, low capacitance (220 pF – 470 pF) capacitor and/or 2–5 MΩ resistor should be installed between the IX6611 COMMON and MCU ground plane, as shown in Figure 4 (Cst, Rst).

Thermal Shutdown

The IX6611 gate driver contains a thermal shutdown circuit to protect the device from damage due to excessive die temperature. When the junction temperature exceeds 150°C, the input signals to the gate driver and the ACL comparator are disabled and the gate driver output is forced low. The device resumes normal operation when the junction temperature falls below 130°C. It is recommended to solder the package bottom pad to the PCB pad tied to V_{EE} to improve package power dissipation.

Layout Considerations

The IX6611 is a high frequency high current driver capable of operating in very noisy environments such as high power motors, inductors, heaters, and other heavy industrial equipment. Close attention should be paid to the PCB layout to maximize noise immunity and performance of the driver.

Figure 5 depicts the recommended decoupling schematics and PCB layout for a IX6611 driving MOSFET. It is recommended to split the decoupling capacitors between the VCC and PVCC pins and locate them as close to the pins as possible. The C3 noise filtering capacitor should be located as close to the ICM input as possible to improve noise immunity. The ground plane should be connected to COMMON and tied to the high current circuit at one point only to avoid high current flowing under the IX6611 gate driver.
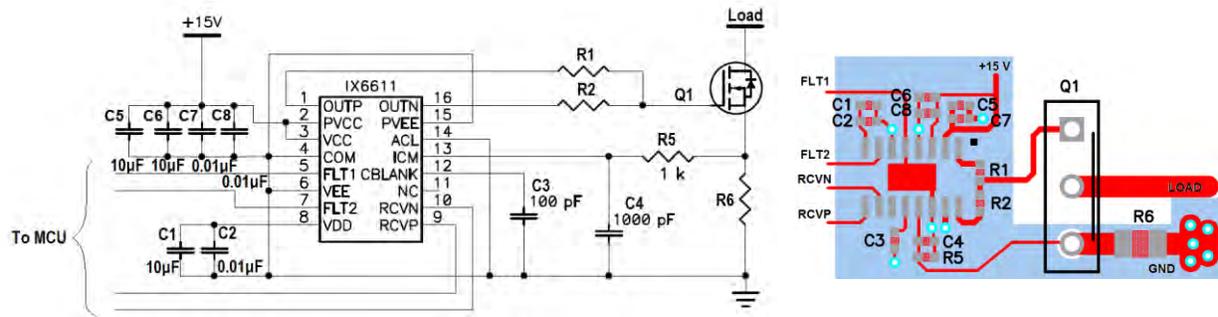
Figure 5. Recommended Decoupling and PCB Layout for IX6611 Driving MOSFET

The internal V_{DD} regulator provides power to the internal low voltage circuits that are referenced to V_{EE}. The regulator is powered from V_{CC} with respect to V_{EE} and its output voltage is referenced to V_{EE}. The C1 and C2 external bypass capacitors accommodate transient currents. When the MOSFET is used as a load, V_{EE} is connected to COMMON and V_{DD} voltage is +5V with respect to COMMON.

Figure 6 depicts the recommended decoupling schematics and PCB layout for an IX6611 driving IGBT. It is recommended to split the decoupling capacitors between the VEE and PVEE pins and locate them as close to the pins as possible. Additional decoupling capacitors may be required between VCC/PVCC and VEE/PVEE to accommodate transient currents.
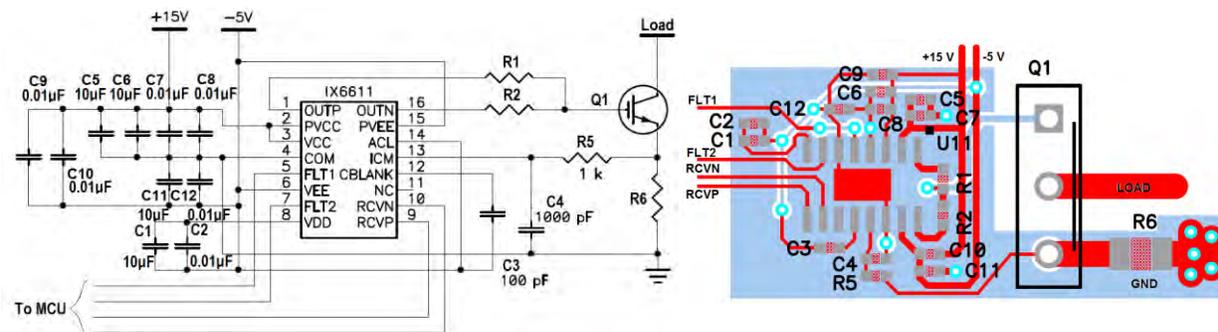
Figure 6. Recommended Decoupling and PCB Layout for IX6611 Driving IGBT

Warranty and Use

IXYS POWER