Digital Control Limits Inrush Current

AC/DC power supplies and rectifiers employ large bulk capacitors. During power-up, these capacitors require large amount of current to charge up resulting in a large inrush current. This inrush current creates limitations in the operation of power devices and interference of those devices with power line and circuit breakers. It also affects the reliability of power system due to overstress caused by instantaneous but huge surge in initial current at power up. Known solutions to limit inrush current [1, 2] require resistors or conventional NTC thermistors which contribute significant power loss and decrease the efficiency. Our approach has two objectives: first, to illustrate advantages of digital power control that overcomes many of the disadvantages of the existing technology and second, to raise interests in digital control of the high power converters, stimulating development of its next generation. **Anatoliy Tsyrganovich, Leonid Neyman, and Abdus Sattar, IXYS Corporation, USA**

IXYS Digital Inrush Current Controller, a novel design that overcomes many of the disadvantages of the existing technology to limit the inrush current in high power AC/DC power supplies and AC/DC rectifiers, combines IXYS digital power control technology with Zilog's 8-bit Z8F3281 MCU to illustrate a unique approach to limit capacitor pre-charge
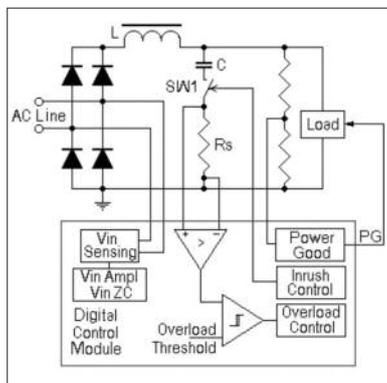

Figure 1: Circuit schematic for digital inrush controller

Figure 2: Digital inrush control timing

current to a predetermined value at each half sine-wave cycle. Capacitor charge is spread over a number of cycles until the capacitor is charged proportionally to a peak value of AC voltage source.

This controller features programmable overload protection and "Power Good" status signal. It is not sensitive to power outage, brownout and ambient temperature variations. It can operate with input voltage range from 80 to 240 V AC and load current up to 3 A. Entire operation process and essential values are fully programmable. The controller may be programmed to 50 Hz, 60 Hz or any other line input frequency operation.

Time-dependent pulse train
Figure 1 shows a conceptual circuit schematic in which the key idea is to provide charge to bulk capacitor in equal increments. Capacitor is charged according to time-dependent pulse train driving the transistor SW1. The pulses are designed in a way to provide substantially equal voltage increment applied to capacitor to keep

peak of charging current about the same value at each cycle. Number of cycles which depends on the capacitor value and the charge current is selected depending on the desired ripples amplitude at the output. The charge current is a function of number of pulses and the timing position with respect to the rectified sine wave.

Figure 2 shows an example of generating the pulse train for SW1. If we can consider N cycles for inrush control then we can split the normalized amplitude of half-rectified sine wave to N segments with increment of 1/N as shown in the Figure 2. During Cycle 1, SW1 is on (conducting) from the time stamp t1 to T thus allowing the capacitor C charge to the voltage proportional to normalized value 1/N. The charging current does not rise instantly because it is a current in serial LC resonant circuit. That shapes the current waveform to the resonant one. The current is rising until capacitor voltage reaches input voltage.

Then current continue its resonant behavior because SW1 is still conducting. No further oscillation occurs because input voltage drops below voltage on capacitor, and then SW1 is off (not conducting). Capacitor remains pre-charged to the voltage proportional to 1/N. In Cycle 2, capacitor C is pre-charged by another voltage increment 1/N in the process similar to Cycle 1. Capacitor C is charged N cycles to the voltage value proportional to the input line voltage.

Principle of operation
Another variable to control inrush current is LC time constant. Capacitor C value depends on desired ripple value. After selecting the capacitor C value, the designer can decrease peak inrush current
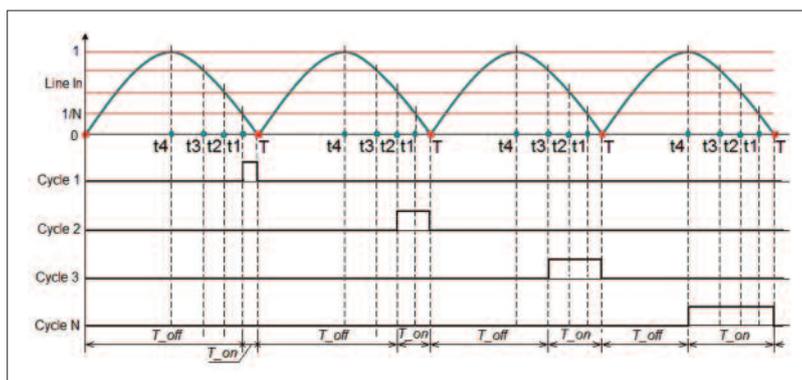
by increasing inductance L. If there are physical limits to L value, the number of cycles N should be used to set the required peak current. Turn ON time for Switch SW1 should be defined for each active cycle.

For cycle 1 in Figure 2, the delay from the zero crossing point (point 0 in Figure 2) to the beginning of turning SW1 on, t1, is denoted as *T_off*. The time between t1 and T, an active time to keep SW1 on is denoted as *T_on*, and the period or cycle duration is denoted as *T*.

Active time *T_on* for each occurrence i is defined as geometrical transform as shown in equation 1:

$$T_{on(i)} = \frac{T}{\pi/2} \mathbf{asin}\,(i/N), \quad where\ i = 1\ldots N; \quad (1)$$

The period T is measured by MCU at initialization. Values of *T_on* are determined by (1) and stored in memory. Values of *T_off* are derived by firmware according to expression 2:

$$T\_off = T - T\_on; \quad (2)$$

Figure 3 illustrates a conceptual algorithm which is executed in MCU Z8F3281 for the first 4 cycles of inrush control. Timing counter value corresponds to time at any given moment of discrete time base provided by the internal clock. The counter first counts from zero crossing to *T_off* value. When the counter reaches *T_off* value, it initiates a *T_on* pulse (black line on Figure 3) which continues till counter reaches *T_on* value finalizing one charging cycle. The rectified power line voltage (blue line) is shown for reference.

Figure 4 illustrates timing position and amplitude of the capacitor C current (red curve) with respect to *T_on* pulses. It is noted that the inrush controller generates
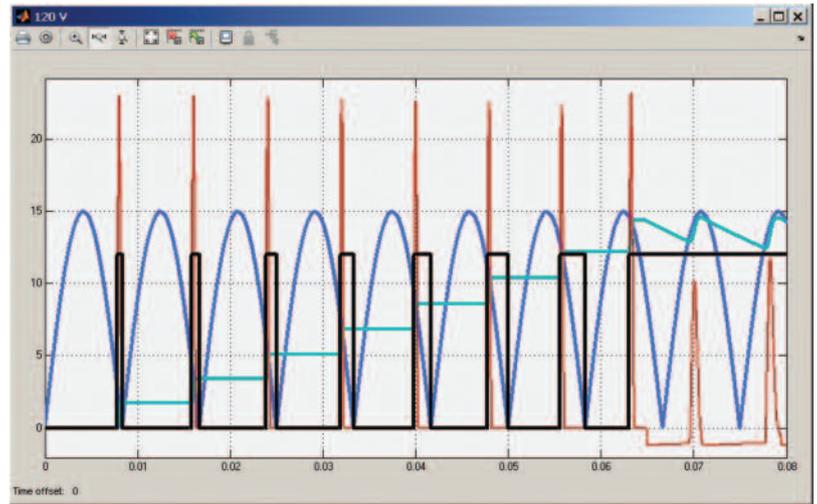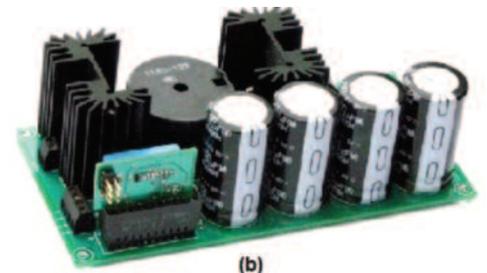

Figure 4: Capacitor C pre-charging (blue – rectified power line voltage, red – power line current, black – on time *T_on* for SW1, green – capacitor C voltage)

Figure 5: MCU module (a) and main power board with MCU module (b)

a single current pulse during each cycle. The capacitor C charge is completed, when input voltage drops below capacitor voltage. The input power line is isolated from the rest of the circuitry by the diode bridge circuit, and inductor discharges into C. Then the switch SW1 is turned off (not conducting) up to the end of the cycle. The algorithm is based on reactive power transfer, hence, losses are limited mostly to those on strain resistance.

Figure 4 also shows that capacitor C pre-

charge is completed at time stamp 0.066 ms. After that, Power Good (PG) signal is generated and load is activated. Capacitor current shows up as negative beginning at time stamp 0.066 ms, because current is sourced from the capacitor when load is activated. Power Good signal can be delayed in respect to end of pre-charge of C to let load stabilize before some other functions are executed. The overload threshold is programmable as well, and it is set to 3.5 A in the current design.

Overload Protection is a valuable feature to protect a device from damage in case of overload. If overload is detected by a comparator, then the MCU disconnects capacitor C from the load by turning off SW1. Also, the PG signal is set to logic low to disable load if possible. Overload protection can be programmed for two modes of operation: (1) immediately shut down the device and wait for user interference and (2) to allow device restart by predetermined number of times.

After initial pre-charging and connecting the load, the MCU may be reconfigured for other power management tasks. For example, it can perform power factor correction (PFC) control and keep track records on device performance, overload conditions, power outages, power brownouts, etc. Based on collected information, the MCU is able to display on
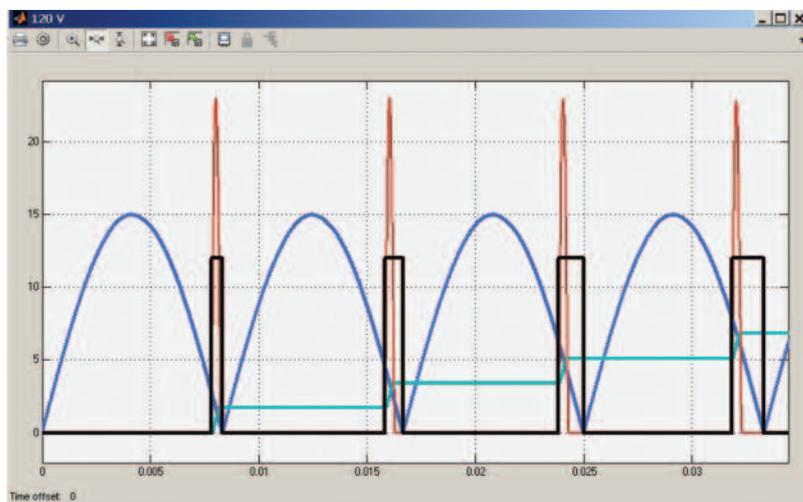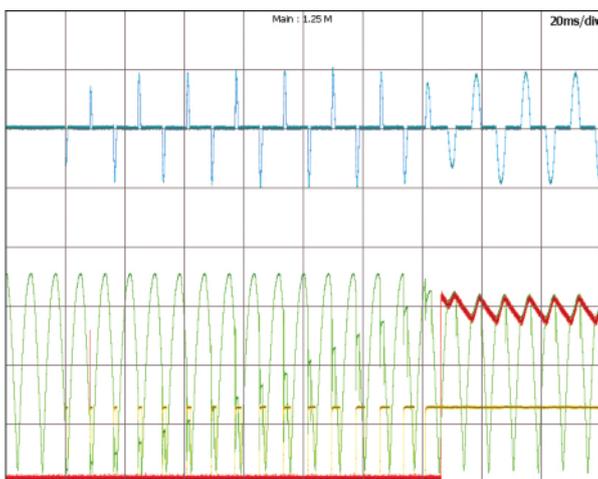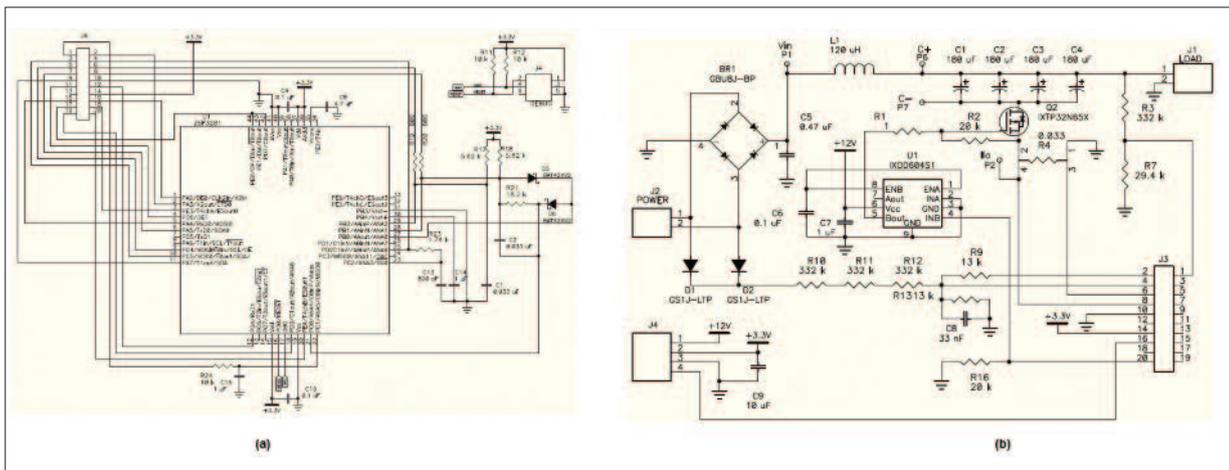

Figure 3: An illustration of *T_on* timing generation (blue – rectified power line voltage, red – power line current, black – on time *T_on* for SW1, green – capacitor C voltage)

(a)   (b)

LEFT Figure 7: Scope snapshot of the digital inrush current control (blue – power line current (10 A/div), red – load voltage (50 V/div), green – rectified input voltage (50 V/div), yellow – SW1 drive signal)

reliability state of the device and supply statistics of system performance.

Digital inrush controller

The digital inrush controller consisting of a MCU module and a main power board is shown in Figure 5. The detailed circuit schematics are included in Figure 6. The MCU module is implemented as an add-on device. The module comprises a connector for MCU programming. The MCU should be programmed before powering the entire system. The MCU module is powered by an auxiliary power supply +3.3 V for the MCU and 12 V for the gate driver applied to the connector J4 on the main power board.

The 2-layer PCB main power board contains the diode bridge and MOSFETs Q1 (SW1), mounted on small heat sinks. Power dissipation is less than 5 W at 375 W output power.

Performance of the design has been verified by several bench tests. A scope snapshot of the test result is shown in Figure 7. Testing confirmed that the inrush current is limited to predefined value and performance of the limiter is quite close to simulation results. The amplitude of the inrush current is limited to the value equal to the input current at maximum load to minimize the negative impact on the AC

line, as well as limit electromagnetic interference (EMI), by selecting of number of inrush current pulses equal 16 and inductor 100 µH. During the test, the AC input line is connected through an isolation transformer as a precaution. The Power Good signal connecting load is generated at rectified voltage zero crossing one cycle after the output capacitor is completely charged (see the red line in Figure 7).

Figure 7 depicts SW1 gate drive pulse T_on time (yellow line) and rectified voltage (green line) at the input of the device. Rectified voltage slightly drops after load is connected due to the limited output power of the isolation transformer used during the test. Blue line depicts line current and red line depicts the load voltage. The system is verified to provide 2.5 A output current at full load or normal operation. Inrush current is limited to 10 A.

Measured efficiency of the inrush control path is 99.5 %. The device is capable of working in wide range of input voltages - from 80V to 240V. Tested power line frequency was 50 Hz and 60 Hz. Dedicated control pulse train was developed for each power line frequency. To apply higher power line voltage, a longer control pulse train is needed in the implementation. For instance, increasing the AC line voltage from 110 V to 220 V requires a double pre-charging time

than that of 110 V to have the same peak inrush current.

Overload protection is based on continuous monitoring of the dynamic current from the bulk capacitor. In case of an overload condition, the current drawn from C instantly increases and the comparator inside the MCU initiates the system overload mode. Overload current threshold, number of overload instances, and the period between overload events are programmable. The system response is being verified successfully by testing an overload condition. The load has been increased to draw an output current of 3.5 A which triggers an overload protection. The system is also tested with continuous overload that results in multiple attempts to restart the system with immediate interruption.

Power Good status is not present in overload conditions. This overload protection is not sensitive to power interruptions, brownout, and temperature variations.

Conclusions

IXYS Digital Inrush Controller offers flexibility in implementing a unique control algorithm that aids in efficient power system. It achieves a high level of efficiency, increased stability, and reliable performance across a wide range of loads. Because of an innovative current measurement algorithm, it allows common input and load grounds. Users can optimize the device for a wide range of input voltages and frequencies. This design provides instant over-current protection, followed by an intervention by the MCU for corrective actions.

Literature

[1] Randhir Singh Malik, William Hemena, Circuit for limiting inrush current to a power source, US6445165 B1, Sep 3, 2002.

[2] Michael Allen, Understanding power supplies and inrush current, Electronic Products, March 2006, pp. 64, 65.