IXI858 / IXI859

Charge Pump, Voltage Regulator, and Gate Driver

By W. Gilbert Bates

1.0 Introduction

The IXI858/859 Charge Pump, Voltage Regulator and Gate Driver is an integration of several key components in an off-line PFC boost regulator using a microprocessor for intelligent power management applications. Specifically these components include a linear voltage regulator with 5V output (IXI858) or 3.3V output (IXI859) to supply power to a micro-controller, a high current non-inverting MOSFET gate driver, a charge pump circuit, trickle charge startup for the device and a 13V regulated output for the MOSFET gate driver. A safety feature is also added to clamp the Vcc voltage so as not to damage the device from over-voltage conditions. The device integrates four independent and dissimilar circuits into one package for a highly integrated power management system.

1.1 General Device Operation

The difficult function of startup is accomplished by using the trickle charging of a capacitor until an under voltage lock out circuit determines the voltage has reached approximately 14 volts. When this level is reached, a linear regulator is enabled to power the microprocessor, allowing it to boot up, and the MOSFET gate driver becomes active. Once the microprocessor is booted and the PFC MOSFET gate drive is operating, charge is pumped from the high voltage PFC circuit back through the V_{SUP} pin, providing power for the microprocessor, gate driver, and any devices attached to the V_{CAP} pin. The internal over voltage zener diode clamp limits the maximum Vcc to 17 volts.

1.2 Pin Description

- V_{CC} (pin 1) Power input from a high voltage source through a current limiting resistor and filter cap. 13V output when charge pump is active and is protected by UVLO Under Voltage Lock Out for low voltage conditions. This pin is clamped (Vclamp) for over-voltage protection by an internal zener diode at 17V.
- V_{OUT} (pin 2) Linear regulated output at 3.3V for the IXI859 or 5V for the IXI858 and is typically used in providing power to a micro-controller.
- Pin 3 is not used.
- IN (pin 4) Used as an input signal to drive the output at pin 5, controlling a power MOSFET in a typical power factor correction application.
- GATE (pin 5) Output for driving external power MOSFET
- GND (pin 6) Ground return.
- V_{SUP} (pin 7) Charge pump input. Receives switching energy from RC and enables / disables charge pump output. Requires low ESR capacitor.
- V_{CAP} (pin 8) Charge pump output to supply external power.

2.0 Typical operation in a Boost / PFC circuit:

The operational characteristics in a typical application can be broken down into three distinct modes: start-up, normal power operation and shutdown. See Figure 2 for boost and power factor correction application.

Figure 1. Device Block Diagram

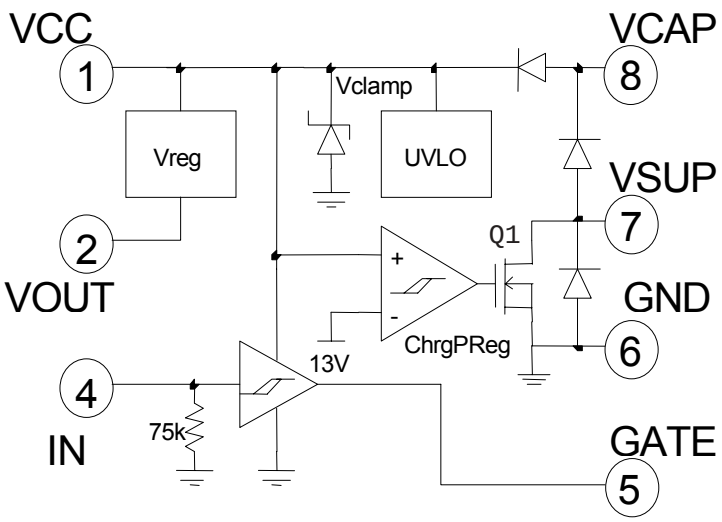
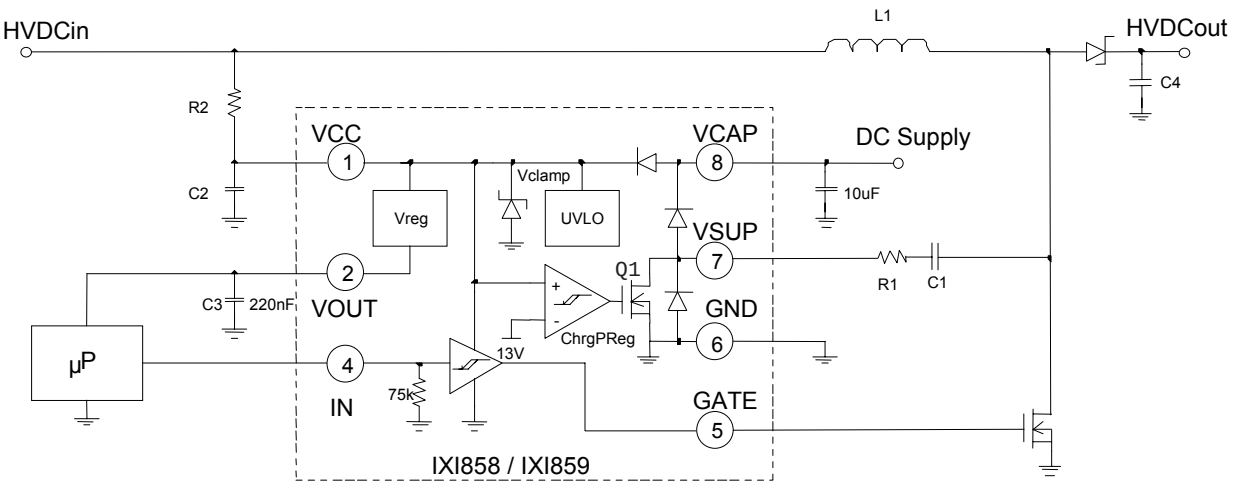


Figure 2. Application Circuit- Boost / Power Factor Correction



When power is initially applied to the circuit in figure 2, C2 will begin to charge toward the HVDCin voltage through R2, as shown during time t1 in figure 3. The voltage across C2 is less than 14.1V, which is the UVLO high voltage point (the startup voltage), and IXI858/859 is in shutdown. In this state, quiescent current of IXI858/859 is less than 6uA, Vout is in a hi-Z state, gate drive output is pulled-low, charge pump regulator and the internal MOSFET switch, Q1, is off. C3 will stay discharged.

The device will enter normal power operation when the voltage on C2 reaches 14.1V. Several events occur simultaneously as the device enters into normal power operation. The internal linear voltage regulator will become active and drive Vout, pin 2, to a regulated voltage of 3.3V for IXI859 and 5.0V for IXI858. The microprocessor will boot-up and the gate driver will actively drive the GATE output on pin 5 to reflect the logic state at input IN on pin 4.

2.1 Determine Startup Components R2, C2

Once the UVLO is released, the initial current out of the Vout pin will be approximately 100mA to quickly charge C3, as shown during time t2, figure 3. Once the regulated voltage is reached, the linear regulator will only supply up to 30mA, shown during time t3, figure 3. The energy required to charge C3 will be supplied from C2 thus there will be a noticeable drop in voltage across C2.

Once C3 is charged, there will be some elapsed time for the microprocessor to actively control the power conversion, driving the PFC circuit. The PFC circuit will then power the VCC pin through the fly-back action of the inductor, L1. C2 therefore must have enough energy stored to power the system while the system is initializing and before beginning to drive the inductor L1.

The loss of charge in C2 due to charge accumulated in C3 is: Q = CV

3.3*C2 for IXI859
5.0*C2 for IXI858

Loss of voltage while the system is initializing and driving the inductor is:

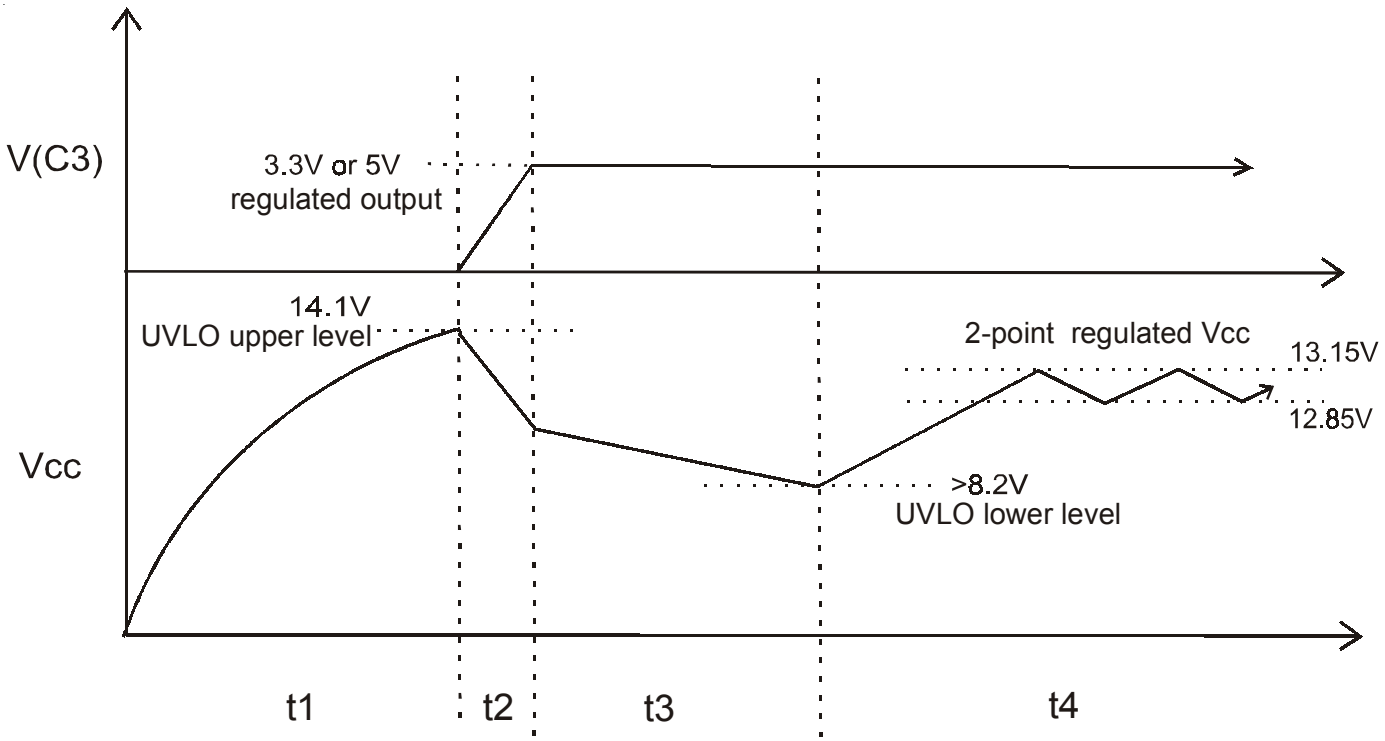
I_{ID}*Time_to_boost/C2

Derived from V = Q/C where I_{ID} is the system current load during initialization. Time_to_boost is the time required to initialize the system plus the time required to charge the inductor. Note that charge in Coulombs has units of Amp*seconds.

Note that once Vout is at regulated voltage, stored energy in C3 does not change. The power is derived from the internal linear regulator.

Size of C2, C3 and R2 must be chosen carefully to avoid accidental shutdown or oscillation during startup.

Figure 3. Startup and Voltage Regulation Waveforms



Now we can express the following:

V1 - V2 - V3 > 8.2V (UVLO lower level)

where $V3 = I_{ID}$*Time_to_boost/C2

Stated in terms of charge:

$(Q1/C2) - (Q2/C2) - (I_{ID}$*Time_to_boost/C2) > 8.2V

where

Q1 = 14.1V * C2 (initial charge)
Q2 = 5V * C3 or 3.3V * C3 (charge transferred to C3)

Thus for the 5V regulator as an example:

$(14.1*C2)/C2 - (5*C3)/C2 - (I_{ID}$*Time_to_boost/C2) > 8.2V

$[(14.1*C2) - (5*C3) - (I_{ID}$*Time_to_boost)]/C2 > 8.2V

Generally stated for both devices:

For IXI858:
$8.2V < (1/C2)*(14.1*C2-5.0*C3)-I_{ID}$*Time_to_boost/C2

For IXI859:
$8.2V < (1/C2)*(14.1*C2-3.3*C3)-I_{ID}$*Time_to_boost/C2

C3 must have a minimum value of 0.2uF to maintain stability. Depending on application and capacitor types, it may be advisable to add 0.01uF or 0.1uf capacitor in parallel to reduce noise on Vout and decouple the linear regulator from the load. From the inequality and solving for C2, one can calculate the minimum capacitor required for C2.

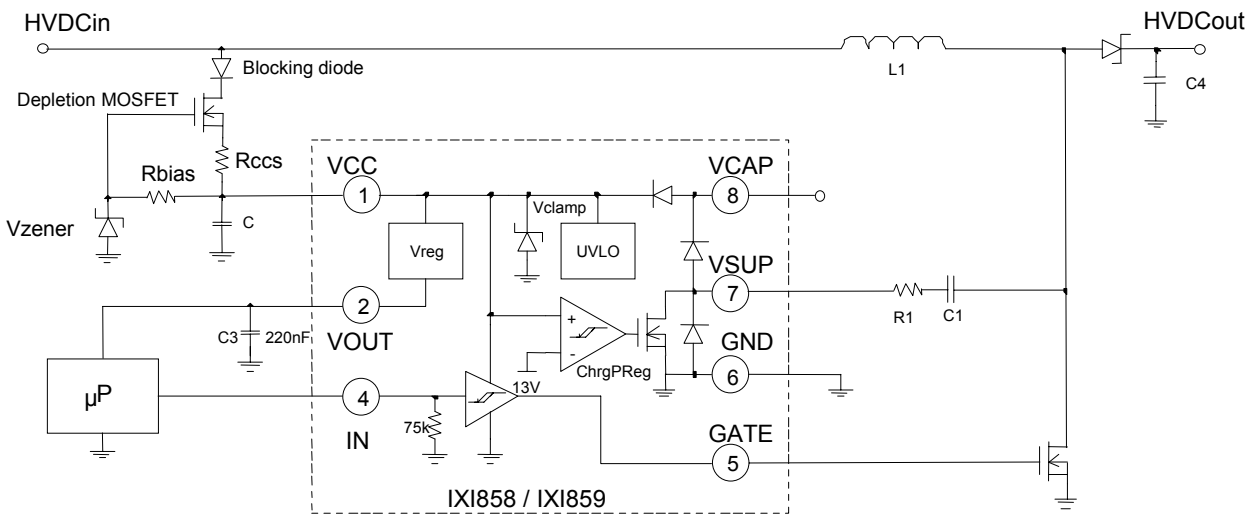
For IXI858:
$C2 > (5.0*C3+I_{ID}$*Time_to_boost)/5.9

For IXI859:
$C2 > (3.3*C3+I_{ID}$*Time_to_boost)/5.9

The selection of R2 is simple but yet very important to the safety of the charge pump device. R2's minimum value is based on the given HVDCin and the resulting current through it. This current must not exceed the minimum system current from the Vout pin plus the maximum allowable current through the internal zener clamp, which is 5mA. Any additional current will cause the voltage to rise across C2 and may result in destruction of the internal zener clamp if too much power is absorbed by it when clamped.

Resistor R2 is used to trickle charge C2, it is not meant to power the system during normal operation. But at the minimum value of R2, we have enough current to power the system. So with a rectified AC input for HVDCin of

Figure 4. Alternative R2, C2 Operation using Constant Current Source



some value, a resulting see-saw effect takes place from where the operating current orginates. At peak AC values of HVDCin, current is sourced through R2, and as the rectified HVDCin approaches 0V, current is sourced through charge pump operation.

Since we don't intend to operate with the internal zener clamped, it is suggested to subtract the maximum allowed current of 5mA through the zener and only use the system operating current to calculate R2.

R2 (minimum) > HVDCin (avg.) / system current

The maximum value of R2 is not really of concern and is selected by the user who decides what the acceptable C2 charge time is during period t1 in figure 3. Keep in mind that during t1 we are only charging C2, the charge pump and system are not operational yet. At the end of t1 we have stored enough charge in C2 to sustain operation to boot the system until the charge pump can take over.

2.2 Alternative R2, C2 operation using a Constant Current Source circuit.

Figure 4 shows a circuit that can be used as an alternative to the Vcc startup components R2 and C2. One feature that might be desired is a low power standby mode in which the processor is allowed to shut down external PFC operation. In this case, R2 and C2 would not be able to provide enough energy by themselves to keep the processor running. Therefore, the processor must stay in an active mode, running the PFC section of the circuit, to provide power back to itself. By utilizing the alternative circuit, enough energy to run the processor is provided which allows it to enter a low power standby mode without driving the PFC section.

Note carefully that there is a caveat in using the alternative constant current source circuit. It was detailed in a previous section that during t2 and t3 in figure 3 there is a time in which the system boots up, before PFC and charge pump operation starts. During this time the Vcc voltage falls from the $UVLO_H$ (14.1V) point down to 12.85V at which point the internal comparator releases the charge pump. The caveat is that too much current is allowed by the constant current source, the Vcc voltage does not fall, and the charge pump is never released by the internal comparator. No charge pump operation will take place and no power will be provided to anything attached to Vcap, pin 8. Therefore the constant current source is viewed as an alternative power supply to the charge pump and everything attached to the Vcap pin should now be tied to some other power source. In other words, use of the alternative circuit disables the charge pump.

As a precaution, the value of Vzener plus the voltage drop of V_{Rbias} must be between $UVLO_H$ (14.1V) and V_{clamp} (17V) so that the internal zener diode clamp is not able to conduct on the high side and $UVLO_H$ can be reached on the low side at start-up. Otherwise the constant current source could clamp the internal Vclamp diode instead of Vzener or $UVLO_H$ will never be reached. Both conditions will result in improper operation.

The addition of Rccs is used to shift power dissipation away from the depletion MOSFET, more so when HVDCin is large. Obviously for the circuit in figure 4, the

source of the depletion MOSFET will be fixed at a value close to that of Vzener. If the value of HVDCin is large then the voltage drop across the depletion MOSFET and resulting power dissipation can be large. Since the general range of power levels for depletion MOSFETs is limited, the use of a Rccs allows a lower power level depletion device to be used by shifting dropped voltage away from it.

The blocking diode is required for when the HVDCin voltage drops below the Vcc pin voltage. This will occur in the case when HVDCin is a rectified sine wave and drops toward zero volts.

2.3 Determine PFC Components R1, C1

The minimum allowable value for R1 is:

$$R1\ (minimum) = Vp/Ip$$

where Vp is the peak voltage for HVDCout. Ip is the peak current allowable to/from the Vsup pin of the charge pump and specified at 1A from the data sheet.

The differential capacitor current for C1 is,

$$I_{C1} = dQ/dt = C1\ (dV/dt)$$

Rearranging for the minimum allowable C1 we have:

$$C1 = I_{C1} * dt/dV$$

Or restated as:

$$C1\ (minimum) = Isystem*Tpd/(Vp-(Vcc+Vd+Vd))$$

where Isystem is the sum of current required by the system, which is the load on the Vout and Vcap pins. Tpd is the switching period of the inductor. (Vp - (Vcc+Vd+Vd)) is the differential change in the voltage across C1over the complete cycle. The two Vd's are the internal diode drops as it charges Vcc. Limit in the datasheet specifies 1.4V for Vd.

If a smaller value of C1 is used, C1 will not transfer enough power onto the Vcc pin to support the system power requirement and will result in collapse of the Vcc voltage.

Too large a value for C1 will result in incomplete charge transfer at end of inductor charge and discharge (fly-back) cycle.

Inductor charge time is controlled by the microprocessor through the GATE pin and the external power MOSFET.

Assuming a complete discharge cycle $di_{CHRG} = di_{DISCHRG}$ and using $di = V_L dt/L$ we can write

$$V_L dt_{CHRG}/L = V_L dt_{DISCHRG}/L \text{ or}$$

$$HVDCin * T_{CHRG}/L = (HVDCout - HVDCin) * T_{DISCHRG}/L$$

The discharge time can then be solved for and approximated by the following equation.

$$T_{DISCHRG} = HVDCin/(HVDCout-HVDCin) * T_{CHRG}$$

The current through the capacitor C1 will be an exponential decay and can be stated as,

$$I_{C1} = Ipk * \exp\{-t / (C1*R1)\}$$

where $t = T_{DISCHRG}$

$$I_{C1} = Ipk * \exp\{-T_{DISCHRG} / (C1*R1)\}$$

In typical application, it is desirable to have less than 1% of residual current after discharge. Thus,

$$\ln(I_{C1} / Ipk) = \ln[\exp\{-T_{DISCHRG} / (C1*R1)\}]$$

$$\ln(0.01) = -T_{DISCHRG} / (C1*R1)$$

Solving for C1

$$C1 = -T_{DISCHRG} / (R1*\ln(0.01))$$

This value for C1 must be larger than the minimum value calculated in the earlier C1 equation.

During normal operation, the excess energy from the PFC will be diverted to ground return via the two-point regulator and the internal MOSFET switch. The two-point regulator actively controls the internal MOSFET switch such that the Vcc remain between 12.85V and 13.15V. When the Vcc voltage drops below 12.85V, the MOSFET switch is turned off and the stored PFC energy is transferred to Vcap and Vcc. When the Vcc voltage exceeds 13.15V, the MOSFET switch is turned on and the stored PFC energy is shunted to ground. Vcap and Vcc voltage will not increase beyond the 13.15V.

Do not forget that energy is pumped into the Vcc and Vcap pins only during the inductor fly-back cycle. The inductor charge cycle produces no useable energy as the charge stored in C2 is routed across the parasitic diode, completing the discharge path, during this time. In other words, only one energy pulse is available during a complete cycle.

Finally, as an example and using figure 7, let us define the pulse discharge waveform with the following parameters. Ip = 1A, maximum peak current allowed, with duration of 1us at which point the current is down to 1% of its original value or 10mA in that amount of time. Also, let us define a peak operating voltage, Vp, as 400V with a nominal switching frequency of 50kHz.

Obviously, we had previously identified the 1A peak current allowed by the device datasheet and the 1% residual current after discharge in a typical application. But what is new here is the pulse duration of 1us. This is arbitrarily selected at 5% of the total switching period. It is arbitrary in the sense that we have not outlined any load conditions on the PFC circuit. But the duration is specific, in a relative sense, to ***light loading*** of the PFC. If the pulse duration was as long as half of the switching period, we would not be able to completely charge C2 if PFC loading was light, resulting in a short inductor charge period. In other words, a relatively short pulse duration assures complete C2 charging under light loads.

So let,

Ip = 1A (maximum allowed for device)

i1 = 10mA (1% residual current)

t1 = 1us (5% of total PFC switch frequency)

Vp = 400V (PFC boost voltage for this example)

So that,

R1 = 400V / 1A = 400 ohms

$C1 = -T_{DISCHRG} / (R1*\ln(0.01)) = 543pF$

$$Q_1 := \int_0^T i(t)\,dt = C1 * V = 217nC$$

where T = 1/f = 1/50kHz = 20us.

Energy C1 = $1/2 * (Q_{C1}^2 / C1) = 43.43uJ$

Power transferred by R1, C1 is:

$P_{C1} = E_{C1} * f = 2.17W$

Power consumed by R1 is:

Figure 5. PFC Waveforms and Circuit

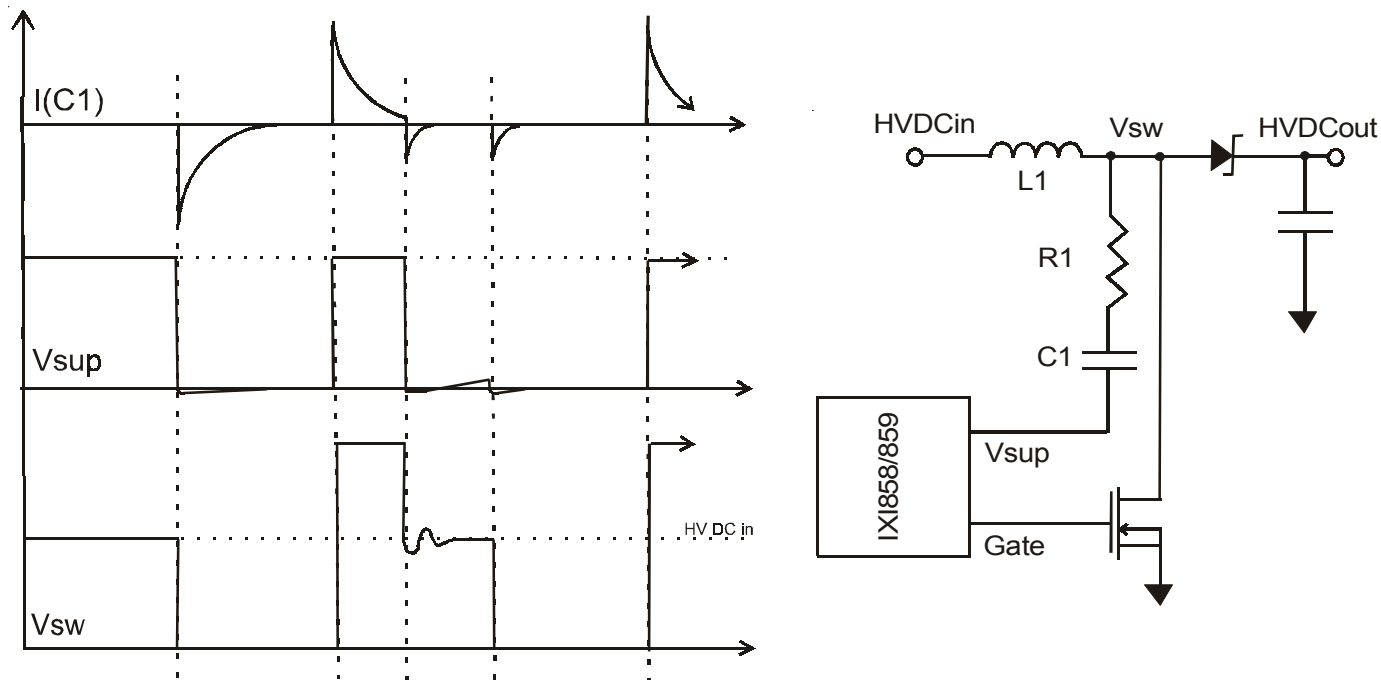
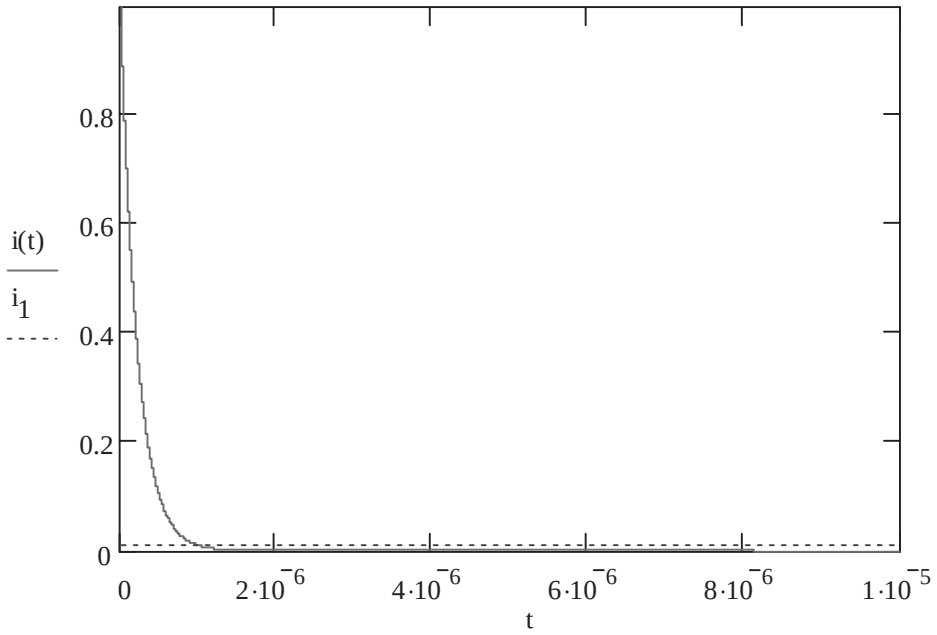


Figure 6. Capacitive Discharge Cycle



$$P_R := \frac{\int_0^T R_1 \cdot i(t)^2 \, dt}{T} = 2.17W$$

3.0 Conclusion

This application note has detailed the IXYS IXI858 and IXI859 capabilities and that it combines many different key primary functions needed for off line PFC / Boost applications for efficient power systems management into one integrated package.

In section 2.1 the application note laid out initial guidelines needed in determining the component values R2, C2 related to start up of the PFC / Boost circuit. We saw that there is an initial start up period in which the device is locked out, waiting to be activated once the upper level lock out voltage point is achieved. Once this point is reached, the device then enters a period in time in which the internal linear voltage regulator powers the microprocessor through the boot-up stage and into normal device operation. It was then indicated that there is a critical stage during the microprocessor boot-up phase in which power must not be bled off too fast before PFC boost operation starts, else the device drops below the lower under voltage lock out point which leads to the collapse of the regulated output voltage and device shut down. No specific example was used to find R2, C2 since microprocessor boot-up time is unique to the application and may mislead the reader to some general assumptions that may not be true for each application about how long it takes to reach normal PFC / boost operation.

Section 2.2 outlined a replacement constant current source circuit for the start-up components R2, C2. One feature that may be desired is a low power standby mode in which the processor is allowed to shut off PFC operation. Since the processor powers itself through PFC operation, a low power standby mode is not possible. So an alternative constant current source circuit was outlined to serve as a replacement for the charge pump section.

After detailing initial start up conditions, the application note then proceeded in identifying the guidelines needed to determine the PFC / boost components R1, C1 in section 2.3. It is noted that the values for R1 and C1 are indirectly found as a result of first knowing PFC circuit operating conditions. That is to say that R1, C1 come as a result of PFC output voltage, inductor switching frequency, and system operating current. Then selecting a small slice of the switching period we find a value of C1. This assures complete charge and discharge cycles for C1 and compensates for light loading of the PFC circuit that might result in short pulse durations. Finally, a general example was used to find R1, C1 based on the absolute maximum values of the parameters found in the IXI858/859 datasheet.

IXYS Corporation
3540 Bassett St; Santa Clara, CA 95054
Tel: 408-982-0700; Fax: 408-496-0670
e-mail: sales@ixys.net
www.ixys.com