

Recent Achievements and Approaches for Further Optimization of High Current Low Voltage Power Semiconductor Components

Andreas Lindemann
IXYS Semiconductor GmbH
Edisonstraße 15, 68623 Lampertheim, Germany
www.IXYS.com

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Abstract

Achievable current density of low voltage power MOSFET components has increased significantly over the past years. Those devices are mainly used in converters for automotive auxiliary drives or renewable energy. The paper outlines state of the art technology and gives an outlook on further development, taking into account the particular requirements of the aforementioned demanding applications.

1 Introduction: Applications

Power electronics has become an indispensable part of automotive electric system [1]. It supplies e. g. adjustable speed fans, water or hydraulic pumps; increasing use can be expected from the introduction of starter generator and 42V system [2] with related units such as electromagnetic valve control. Compared to known industrial power electronics in a similar power range of several Kilowatts, the current levels in battery supplied automotive systems are high; to achieve a compact power section consequently a high current density of the semiconductor devices is mandatory. Operational conditions of converters — frequently tempered by the coolant of the combustion engine — are characterized by a wide temperature range with maximum heatsink temperature reaching some $T_S = 110^\circ C$. This has an impact on component reliability, which is requested to be extremely high for the time span of cars' life expectancy, thus leading to particularly demanding reliability criteria [3].

Cars powered by fuel cells show a link to other applications employing low voltage high current switches — being related to renewable energies: Fuel cell systems gain importance for storage and transportation of electrical energy, especially generated from variable sources such as wind parks [4]. The output voltage of photovoltaic arrays depends on the number of series connected cells; system configurations using a boost converter to transform voltage of solar generator to a higher level — e. g. to generate a mains like AC output with a subsequent inverter — thus are frequently met. Efficient operation of converters in the field of renewable energy is important, leading to the requirement that the power semiconductor switches should operate with minimum losses [5].

2 State of the Art

Figure 1 shows the development of current density — current per volume — of isolated power semiconductor components with MOSFETs over the last years: The devices listed up to 2002 currently are in production while the types in 2003 are under development, their characteristics thus tentative.

The arrangement in the figure refers the sum of DC current capabilities I_{D80} of all switches in the component at a case temperature of $T_C = 80^\circ C$ according to

$$I_{D(T_C)} = \sqrt{\frac{T_{Jmax} - T_C}{R_{DSon}(T_{Jmax}) \cdot R_{thJC}}} \quad (1)$$

with $R_{DSon}(T_{Jmax})$ being the chips' on state resistance at maximum junction temperature and R_{thJC} the thermal resistance from junction to case. To permit comparison of the different values, components with a blocking voltage $U_{DSS} = 100V$ have been chosen for reference; current capability of devices with different blocking voltages has been related, assuming a dependence of on state resistance from blocking voltage

$$R_{DSon} \sim U_{DSS}^{2,6} \quad (2)$$

To obtain current density as logarithmically scaled on the vertical axis, the sum of switch current capabilities I_{D80} is divided by the volume V of device package; this includes the volume of plastic body itself and — in case the device provides leads for soldering into a printed circuit board — its prolongation over the wide portion of the leads which will determine the distance between plastic body of assembled device and board.

Table 1 gives some details about the parts depicted in figure 1: The type designation is assigned to the aforementioned ratings U_{DSS} and I_{D80} per switch, if applicable including the calculated reference; further, circuit and component dimensions are indicated as well as kind of chips and packages.

Table 1: technologies and basic ratings and characteristics of isolated high current low voltage power MOSFET components

modules				
type	VMO650-01F	VMM650-01F	VWM350-0075P	
MOSFET	planar	large planar	trench	
U_{DSS}	100V	100V	75V (ref: 100V)	
I_{D80}	650A	500A	275A (ref: 185A)	
circuit	single switch	phaseleg	sixpack	
package	module	low L_p module	low profile module	
dimensions	$110 \cdot 62 \cdot 30mm^3$	$110 \cdot 62 \cdot 30mm^3$	$93 \cdot 40 \cdot 17mm^3$	
discrete components				
type	FMM150-0075P	FMM300-0055P	FMM200-0075P	GWM160-0055P3
MOSFET	trench	trench	trench	trench
U_{DSS}	75V (ref: 100V)	55V (ref: 100V)	75V (ref: 100V)	55V (ref: 100V)
I_{D80}	125A (ref: 85A)	230A (ref: 100A)	170A (ref: 115A)	125A (ref: 55A)
circuit	phaseleg	phaseleg	phaseleg	sixpack
package	ISOPLUS i4 TM		ISOPLUS i4 TM (DAB)	ISOPLUS TM DIL1000
dimensions	$(21 + 2, 24) \cdot 20 \cdot 5mm^3$			$(25 + 4) \cdot 37,5 \cdot 5mm^3$

At a first glance, figure 1 illustrates a dramatic increase of current density by a factor of more than 30 over nine years. The following more detailed observations can be made:

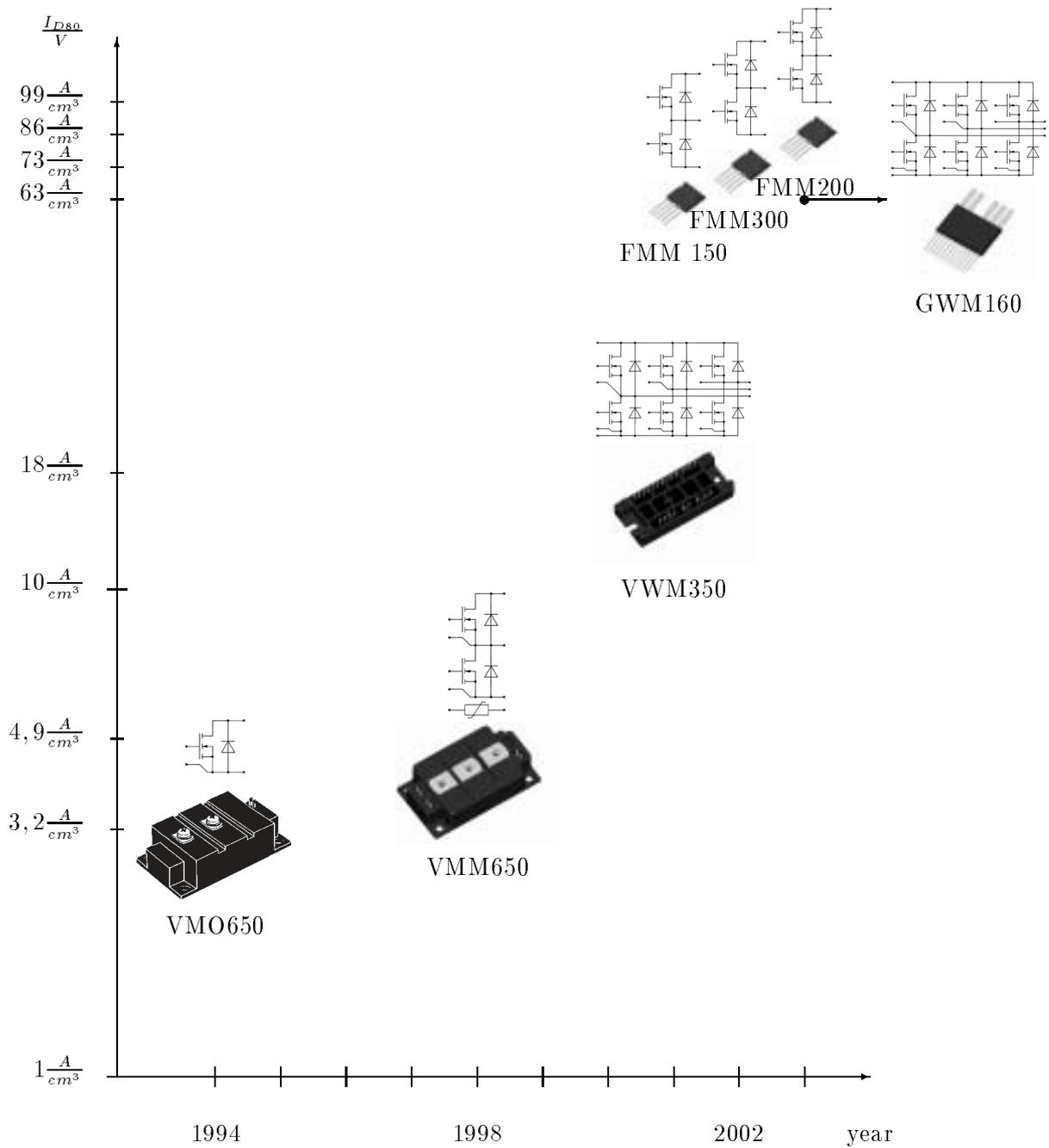


Figure 1: development of current densities of isolated high current low voltage power MOSFET components

- Current density of isolated discrete components generally is higher than of modules. This is obvious comparing the group of discretets (FMM, GWM) with the group of modules (VMO, VMM, VWM) in figure 1, in particular also with regard to FMM150 and VWM350, both using the same chip technology and generation.

The root cause for this is packaging technology.

- The degree of integration — thus current density — could be increased in the course of time within each of those groups. The reason is two-fold:

Progress in MOSFET technology permits to reduce on state resistance R_{DSon} , leading to higher current capability according to equation 1. This becomes visible e. g. in the higher current density of FMM300 compared to FMM200, using the same packaging technology but subsequent chip generations.

An optimization of package design, matched to the particular MOSFET devices, also contributes to this effect as the difference between FMM200 and FMM300, both using the same generation of MOSFETs, but FMM200 in a redesigned internal package layout, shows.

- The continuous development permits the incorporation of increasingly complex topologies into the same kind of package. This is obvious for the modules, having undergone the development from single switch VMO via phaseleg VMM up to three phase bridge VWM for AC motor drives; with the introduction of DCB based ISOPLUSTM packaging technology, the same could be achieved for isolated discrete devices, where the phaselegs FMM will be complemented by a three phase bridge GWM.

It should be noted that current density is lower for devices incorporating a more complex topology and using the same chip technology, cf. FMM300 vs. GWM160. The reason is the necessity to integrate interconnections which are situated outside of the devices with more simple topologies. The fact that those interconnections needn't be realized separately can however be expected to overcompensate this effect on system level, making the system most compact, using devices with highest degree of integration.

The following sections 3.1 and 3.2 will more in detail deal with MOSFET and in particular packaging technology which have been explained to be the root causes for the development outlined in figure 1.

3 Technological Background

3.1 MOSFET Technology

Several steps in chip technology have contributed to the development as outlined in figure 1. According to table 1, initially planar MOSFETs have been used. Those devices with a structure as sketched in figure 2 (left) are derived from MOSFETs with higher blocking voltage; to optimize turn off behaviour of the intrinsic body diode — which is essential e. g. in bridge circuits such as for induction motors —, the devices become irradiated. Characteristics of this kind of chips have been improved by a new generation which also comprised chips with a considerably large area of $150mm^2$, designated as "large planar" MOSFETs in the table.

A fundamental increase of devices' current density is tied up with the introduction of trench MOSFETs. Unlike planar MOSFETs with a basically horizontal channel leading to JFET effect between the cells, they provide a vertical channel as schematically depicted in figure 2 (right). This principle is known for years [6]; several subsequent generations have been developed, improving electrical characteristics — in particular on state resistance R_{DSon} — by more narrow trench structures and reduced cell pitch [7].

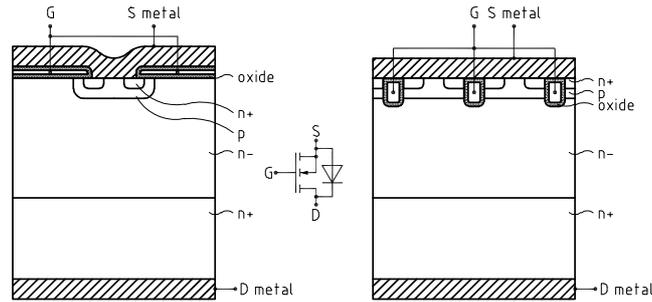


Figure 2: cross section of a planar (left) and a trench MOSFET (right)

3.2 Packaging Technology

The package protects the chips against environmental influence, it provides leads for the electrical connections and a thermal interface towards heatsink. The modules [8] and isolated discretes [9][10] under question in this paper are based on ceramic substrates with metal layers bonded on top and bottom — typically DCB with copper sheets on Al_2O_3 ceramics. The chips and at least parts of the external leads are soldered onto the structured top metallization of this substrate; electrical connections from the top sides of the chips are effectuated by aluminium wire bonds. The bottom metallization of the substrate is intended to be pressed to heatsink for thermal coupling. The remaining outer surface of the module package is a kind of plastic frame, being filled with silicon gel and possibly additional epoxy, while discrete packages' body consists of solid, moulded plastic. This is a reason for the difference in current density between the groups of modules and discretes noted in section 2 — the single layer of moulding compound typically has a smaller volume than the multiple components of module package, which in addition provides means for screwing down to heatsink, being substituted by external spring clips in case of isolated discretes.

Conventionally DCB substrates with a ceramic thickness of $0,63mm$ have been employed as base for modules, which has been maintained for the isolated discretes. The latest developments in the field of modules and discretes aim at a reduction of the related thermal resistance R_{thJC} according to equation 1: VWM350 and GWM160 use $0,38mm$ thick ceramic layers. Their isolation voltage of at least several hundreds of Volts is sufficient for low voltage components. Thermal resistance from junction to case R_{thJC} has been shown to be some 30% better, while thermal resistance from case to heatsink R_{thCS} remains unchanged; measurements are in good accordance with thermal modelling.

The following subsections deal with several aspects of packaging technology which have shown to be of particular importance for the use of high current low voltage power semiconductor components in applications such as mentioned in section 1: Parasitic effects — in particular mounting resistance as explained in section 3.2.1 and parasitic inductance according to section 3.2.2 — affect operational behaviour of a circuit increasingly when operating voltage decreases and current level increases. In practice both — which are treated separately for sake of clearness — of course superpose on each other. Additionally, parasitic coupling capacities may be taken into account, which however have been shown to remain relatively low for components with isolation by ceramic substrates [11]. Moreover, section 3.2.3 covers some essential aspects and approaches how power electronics has been and may in future be further enabled for operation under harsh environmental conditions as outlined in section 1 with reference to automotive applications.

3.2.1 Mounting Resistance

The schematic of a phaseleg consisting of two MOSFETs T_1 with D_1 and T_2 with D_2 in figure 3 (left) is complemented by resistances which result of the aforementioned electrical interconnections through leads, wire bonds and substrate metallization. Assuming a current flow $I_{D1} > 0$ through MOSFET T_1 being turned on, a voltage drop

$$U_{L_+L_1} = (R_{D1} + R_{DSon} + R_{S1} + R_{L1}) \cdot I_{D1} \quad (3)$$

occurs between L_+ and L_1 which may be significantly higher than $R_{DSon} \cdot I_{D1}$ due to the fact that on state resistance of today's trench MOSFETs can be sufficiently low in the order of magnitude of few Milliohms to meet $R_{DSon} \approx R_{D1} + R_{S1} + R_{L1}$ for high current devices.

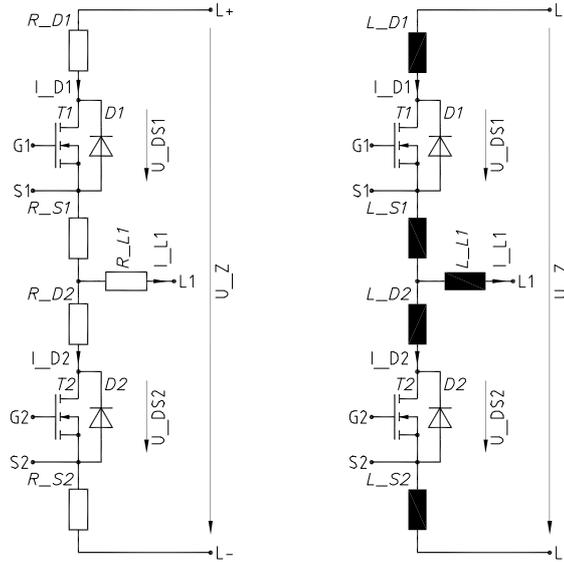


Figure 3: phaseleg circuit with mounting resistances (left) and parasitic inductances (right)

The indication of characteristic value R_{DSon} in device data sheets refers to the voltage drop which can be measured between the terminals, i. e. gives $R_{DSon,datasheet} = \frac{U_{L_+L_1}}{I_{D1}}$ according to equation 3 or the corresponding value for T_2 in case the sum of mounting resistances is higher in its current path $R_{D2} + R_{S2} > R_{D1} + R_{S1}$. This indication however is not accurate for the calculation of MOSFET power loss or current rating respectively according to equation 1. Contrary, a considerable portion of losses $P_{VM} = (R_{D1} + R_{S1} + R_{L1}) \cdot I_{D1}^2$ occurs outside the chips, heating up parts of the package to an extent which is difficult to exactly quantify:

- Losses in the terminals may be dissipated to heatsink in the same way as losses in the chips in case the leads are directly joint to the substrate. Further, a heatflow may occur between the leads and the busbar, board or cable they are externally connected to. Ideally those external connections are designed to remain cool during operation, which in a DC approach is a question of cross section, heat dissipating surface and ambient temperature; this way they would not additionally heat up the device and may even contribute to cooling of its leads.

To prevent the terminals from overheating, an additional package current rating — such as maximum I_{RMS} per terminal — may be indicated. Its definition depends on the kind of terminal; a reasonable limit for solder pins would e. g. make sure that temperature of their solder joint to an appropriately designed — i. e. high current — board remains

significantly below melting point of the solder. While package current limitation I_{RMS} often is above chip current limitation — cf. equation 1 — in automotive applications with high heatsink temperatures, it may be a more severe constraint in other low voltage converters such as for renewable energy systems.

- Another limiting factor for the device current rating I_{RMS} may be the wire bond connections. Their resistance and thus power losses generated in them depend on length and cross section — thus also on the number of paralleled wires. Temperature results of power losses and ambient conditions: While heat dissipation from the bond wires towards isolating silicon gel or moulding compound is low, heat transfer may occur from the chips to the wire bonds, from the wire bonds to the cooled substrate and from the wire bonds to the terminals or vice versa. While extremely high current levels may cause the wires to fuse, a reasonable current limit I_{RMS} will take into account ageing effects limiting device reliability [12].

As a remedy it has been proposed to replace at least parts of the wire bonds in the main current paths by solid metal clips as known from thyristor devices or to optimize wire bonding as described below for a new high current device.

- The current paths in the substrate metallization also contribute to power losses P_{VM} , however typically do not limit device current capability because of the thermal coupling of substrate to heatsink.

Figure 4 depicts a new device which is currently under development [13]: As mentioned in section 2 it is a discrete device incorporating a three phase MOSFET bridge. Several details visible in the cut off view show how a dedicated design for a low voltage high current component can take the respective particularities into account and thus lead to an optimized solution:

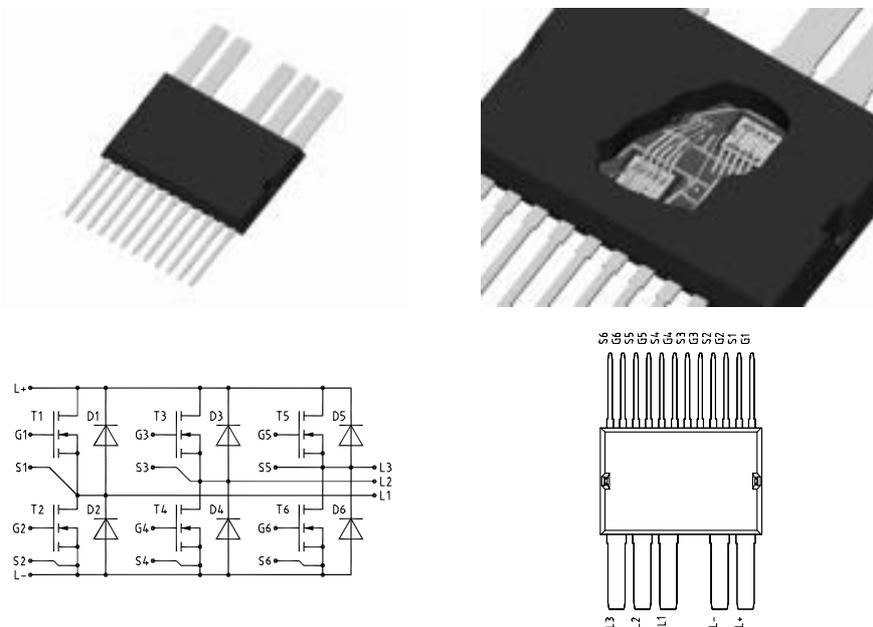


Figure 4: external view (top left), enlarged cut-off view (top right), schematic (bottom left) and pinout (bottom right) of proposed GWM160-0055P3 component

- The high current terminals L_+ , L_- , L_1 , L_2 and L_3 have a large cross section due to their

width of 4mm. Further their excessive heat up is prevented by thermal coupling to the substrate.

- Contrary to most standard discrete devices, a high number of five wire bonds can be placed on the source of the chips, leading to a considerable cross section of the wire bond connections in the main current paths. The wires are short with a length in the order of magnitude of 1cm between chip and substrate, where all of them end on a conductor which is thermally coupled to heatsink through the ceramic substrate. This way losses in the wires and wire temperature are minimized.

3.2.2 Parasitic Inductance

Figure 3 (right) shows parasitic inductances being distributed in the phaseleg circuit with basically the same arrangement as mounting resistances. In voltage source inverters — this circuit is suitable for — the voltage between the terminals L_+ and L_- of the intermediate circuit U_Z is kept as constant as possible by capacitors. To determine the effects of parasitic inductances, a commutation interval is considered in the following where the load current is assumed to have a constant positive value $i_{L1}(t) = I_{L1} > 0$.

There is the general relationship between the currents:

$$i_{D1}(t) - i_{D2}(t) = i_{L1}(t) = I_{L1} > 0 \quad (4)$$

Before the commutation, the load current flows via T_1 :

$$i_{D1}(t) = i_{L1}(t) = I_{L1} \quad \text{and} \quad i_{D2}(t) = 0 \quad (5)$$

When T_1 turns off, the current will commutate from T_1 to the intrinsic free wheeling diode of T_2 :

$$\frac{di_{D1}}{dt} - \frac{di_{D2}}{dt} = \frac{di_{L1}}{dt} = 0 \quad \Rightarrow \quad \frac{di_{D1}}{dt} = \frac{di_{D2}}{dt} < 0 \quad (6)$$

Calculating the loop voltage then leads to

$$U_Z = (L_{D1} + L_{S1})\frac{di_{D1}(t)}{dt} + u_{DS1}(t) + (L_{D2} + L_{S2})\frac{di_{D2}(t)}{dt} + u_{DS2}(t) \quad (7)$$

and thus

$$u_{DS1}(t) + u_{DS2}(t) = U_Z - (L_{D1} + L_{S1} + L_{D2} + L_{S2})\frac{di_{D1}(t)}{dt} \quad (8)$$

Considering $\frac{di_{D1}(t)}{dt} < 0$ according to equation 6, this means that the series connection of semiconductor devices T_1 and T_2 has to block a voltage being higher than of intermediate circuit. Assuming that the commutation of the current starts when T_1 has taken over blocking voltage and the free wheeling diode of T_2 starts conduction — leading to $u_2(t) \approx 0$ — an overvoltage peak at the device turning off occurs according to:

$$\hat{U}_{DS1} = U_Z - (L_{D1} + L_{S1} + L_{D2} + L_{S2})\frac{di_{D1}(t)}{dt} = U_Z - L_P \cdot \frac{di_{D1}(t)}{dt} \quad (9)$$

This overvoltage peak is dependant on the sum $L_P = L_{D1} + L_{S1} + L_{D2} + L_{S2}$ of all inductances between plus L_+ and minus L_- of constant voltage intermediate circuit.

It can be shown that the same result as above is obtained in case a possible coupling between certain inductances is taken into account, as may occur depending on the geometrical arrangement. The described approach can of course also be applied for the inverse commutation from the diode of T_2 to the transistor T_1 and for the opposite direction of load current I_{L1} .

An example shows why consideration of parasitic inductance may be essential in low voltage high current converters: It is assumed that in a $U_Z = 12V$ system a current of $I_{L1} = 100A$ is commutated within 50ns; parasitic inductance shall be $L_P = 20nH$. Thus equation 9 results in

$$\hat{U}_{DS1} = 12V + 20nH \cdot \frac{100A}{50ns} = 52V \quad (10)$$

Rated voltage of the MOSFETs must not be exceeded which means that under the above conditions a device rating of 55V would be just sufficient.

For an appropriate design parasitic inductances of the whole circuit — i. e. of the MOSFET device itself and of DC link — should be taken into account. [14] proposes the indication of parasitic inductance as a characteristic value L_P for the device. The components this paper deals with exhibit values in the order of magnitude between few Nanohenries and few tens of Nanohenries; a dedicated geometry inside the component may help to keep parasitic inductance low, as has been applied in the construction of VMM module, cf. table 1. Complementary parasitic inductance of DC link strongly depends on its layout; in particular high current power sections may reach considerable values because of the length of current paths related to their mechanical dimensions. Additionally the DC link capacitors, being intended to act as voltage sources, contribute to parasitic inductance.

A second effect of parts of parasitic inductance should be noted: In case the gate driver uses a portion of source main current path, this will result in an unwanted coupling of gate control and load current. Assuming e. g. that MOSFET T_2 is intended to be turned on by a positive gate voltage between G_2 and L_- , the subsequent $\frac{di_{D2}}{dt} > 0$ will lead to a reduction of gate voltage by $L_{S2} \cdot \frac{di_{D2}}{dt}$. This can be avoided by separating current and control paths, thus using auxiliary source terminals — S_2 in the example referencing figure 3 (right).

Again figure 4 shows measures to minimize the aforementioned parasitic effects by device design dedicated to low voltage high current applications: Parasitic inductance between DC link terminals L_+ and L_- is minimized by placing the respective pins and conductors close together. The flat geometry of the discrete component further guarantees short current paths with hardly any extension into third dimension. Additionally disturbance of MOSFET control by load current is avoided providing separate auxiliary source terminals associated to the respective gate terminals as specified in the pinout.

3.2.3 Reliability

As mentioned in section 1, reliability requirements for automotive applications are defined in documents like [3]; general test methods and conditions can be found e. g. in [14]. Failure mechanisms related to load cycling have already been mentioned in section 3.2.1.

There are several other failure mechanisms caused by temperature cycling:

- Conventional, non-isolated discrete components such as TO220 may exhibit chip crack or delamination of solder joint between silicon chip and copper carrier because of the mismatch between thermal expansion coefficients α of silicon and copper, leading to mechanical stress — see table 2.

For the isolated components based on ceramic substrate, this paper deals with, chip crack is not a typical failure mechanism caused by temperature cycles. Delamination of the solder joint between chip and substrate will be experienced significantly later — i. e. after a higher number of cycles or at higher average temperature and temperature difference respectively — due to the better match of silicon's and DCB's thermal expansion coefficients α .

Low temperature joining techniques have been developed [15] which might in future substitute the conventional soldering process, further reducing the probability of the latter failure mechanism to a minimum.

- Delamination of a large area solder joint between DCB and base plate may occur in case of devices with base plate.

All devices under question in this paper are based on ceramic substrates without additional base plate, which excludes this failure mechanism and additionally saves space, weight and cost.

- Further, an interruption of current path is possible, e. g. by mechanical destruction of the joint of a terminal to the substrate or of wire bonds.

Table 2: thermal expansion coefficients α of silicon and different chip carriers, resulting approximate change of length Δl for a length of $l = 10mm$ and $\Delta T = 100K$ according to $\frac{\Delta l}{l} = \alpha \cdot \Delta T$

$\frac{\alpha}{10^{-6} \frac{1}{K}}$	for	at	$\frac{\Delta l}{\mu m}$
2,53	silicon	$T = 25^{\circ}C$	2,53
7,40	DCB	$50^{\circ}C \leq T \leq 200^{\circ}C$	7,4
16,80	copper	$0^{\circ}C \leq T \leq 100^{\circ}C$	16,8

A new composition of direct metal bonded ceramic substrates — DAB — gives reason to expect a further increase of temperature cycling reliability of the substrate itself as explained in the following section.

4 Outlook: DAB Direct Aluminium Bonding

As explained in section 3.2, most of the high current low voltage power semiconductor components outlined in figure 1 use DCB — direct copper bonded — ceramic substrates. FMM200 is an exception: It is a first discrete device currently being under development, using a DAB — direct aluminium bond — substrate. Like DCB substrates this is based on an Al_2O_3 ceramic, however not being bonded with copper but with aluminium sheets on its top and bottom sides. Table 3 indicates some material properties of copper and aluminium for comparison of the two types of substrates:

Table 3: electrical, thermal and mechanical characteristics of copper and aluminium

	specific el. resistance $\frac{\rho}{\Omega \cdot m}$	therm. conductivity $\frac{\lambda}{\frac{W}{m \cdot K}}$	therm. capacity $\frac{c}{\frac{J}{kg \cdot K}}$	specific weight $\frac{\delta}{\frac{kg}{m^3}}$
copper	$1,6 \cdot 10^{-8}$	398	417	8890
aluminium	$2,4 \cdot 10^{-8}$	208	892	2700

Electrical resistance

$$R = \rho \frac{l}{A} \quad (11)$$

of a conductor with a length of $l = 25mm$ and a cross section of $A = 10mm \cdot 0,3mm$, where $0,3mm$ is the thickness of the layer, will be $R = 200\mu\Omega$ for DAB aluminium, which is $67\mu\Omega$ higher than for DCB copper metallization. It depends on the total on state resistance of the device whether this increase is of some significance or neglectable.

Thermal resistance from junction to case for a chip with an area of $25mm^2$ will be some $R_{thJC} = 1 \frac{K}{W}$. A detailed estimation of thermal resistance with the heat flowing through the different layers, taking into account thermal conductivities λ of copper and aluminium according to

table 3 and assuming heat spreading with an angle of 45° in the metal layers, results in thermal resistance of DAB being some $0,045 \frac{K}{W}$ — thus less than 5% — higher than of DCB, which is well within the typical tolerances of thermal joint of devices being assembled on heatsink using heat transfer paste. The reason for this small change is that the portion of thermal resistance in the metal sheets is low compared in particular to the ceramic layer's.

Mechanically, a minor weight difference of some $1g$ can be expected between a DAB and DCB based FMM device — cf. figure 1 and table 1 — according to

$$m = \delta \cdot V \quad (12)$$

where the volume is $V = 2 \cdot 0,3mm \cdot 17mm \cdot 16mm$ for the two metal layers of $0,3mm$ thickness and based on package geometry.

While basic electrical, thermal and mechanical properties of DAB thus are very similar to DCB's, an even increased level of reliability in case of high amplitude temperature cycling can be expected from DAB. The reason is that the ceramic is exposed to significantly less mechanical stress by the bonded aluminium layers, preventing it from cracking. As an experimental proof, DAB substrates are currently undergoing extensive temperature cycling tests, the results of which are intended to be published in a later paper.

Further, components manufactured on DAB base shall provide an increased strength of the joints between wire bonds and substrate metallization, which in case of DAB both consist of aluminium. This promises to minimize probability of the last failure mechanism listed in section 3.2.3. The first DAB based component FMM200 consequently is intended to be a vehicle for extensive reliability testing on component level.

5 Conclusion

Low voltage power MOSFET components have rapidly developed, thus significantly contributing to efficiency, system integration and reliability of low voltage high current converters such as battery supplied automotive inverters or power electronics for renewable energy systems. Characteristics of state of the art components have come closer to ideal switches'; this leads to parasitic effects, previously being neglectable, attracting more attention. Approaches for further optimization which are pursued in the course of current research and development work have been described — e. g. aiming at the introduction of a high current three phase bridge for drives, integrated in a single, compact, isolated device, or the use of new materials.

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