DC to DC Synchronous Converter Design
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IXAN0068

Modern power electronics products require small size and lighter weight of power electronics parts. Filter inductor and capacitor sizes must be small. With the small filter, the switching semiconductor devices must have small switching loss. And heat sink also must be reduced. For the safe operation with the small heat sink, the switching semiconductor devices must have small conduction loss. IXYS developed new generation of Trench MOSFET (Trench2^{TM}), which has small gate charge and low on-resistance. The MOSFET will be well suited for high power applications of synchronous DC to DC converters used in various systems. The MOSFET is rugged and has avalanche energy capability.

Table 1: Few Examples of IXYS TrenchT2^{TM} N-Channel Power MOSFETs

Part Number	Vdss (max) (V)	Id @ Tc=25C (A)	Rds(on) @ Tj=25°C (Ω)	Ciss (pF)	Qg (nC)	trr @ Tj= 25°C (ns)	R(th)JC (°C/W)	Pd (W)	E_{AS} (mJ)	Package Type
IXTA220N04T2	40	220	0.0035	6500	112	45	0.42	360	600	TO-263
IXTP220N04T2	40	220	0.0035	6500	112	45	0.42	360	600	TO-220
IXTA90N055T2	55	90	0.0084	2670	42	37	1.0	150	300	TO-263
IXTP90N055T2	55	90	0.0084	2670	42	37	1.0	150	300	TO-220
IXTA110N055T2	55	110	0.0066	3060	57	38	0.82	180	400	TO-263
IXTP110N055T2	55	110	0.0066	3060	57	38	0.82	180	400	TO-220
IXTA200N055T2	55	200	0.0042	6800	109	49	0.42	360	600	TO-263
IXTP200N055T2	55	200	0.0042	6800	109	49	0.42	360	600	TO-220
IXTA70N075T2	75	70	0.012	2580	46	48	1.0	150	300	TO-263
IXTP70N075T2	75	70	0.012	2580	46	48	1.0	150	300	TO-220
IXTA90N075T2	75	90	0.010	3100	54	50	0.82	180	400	TO-263
IXTP90N075T2	75	90	0.010	3100	54	50	0.82	180	400	TO-220

DC-to-DC Synchronous Converter Design:

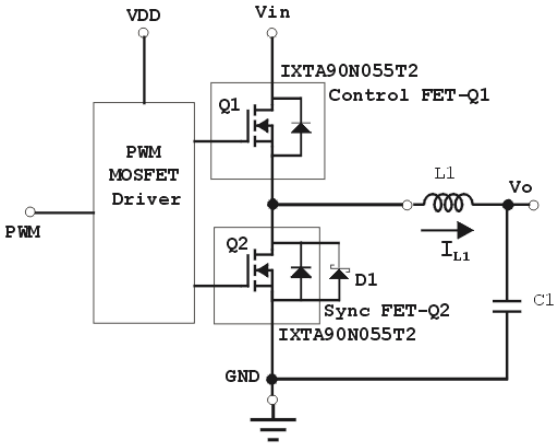

Figure 1: Synchronous Buck Converter using IXYS TrenchT2^{TM} Power MOSFET

In Figure 1, the Q1 is called the high-side or control FET and Q2 is called the low-side or sync FET applied in a step-down DC to DC synchronous converter application. The ratio *Vo*/*Vin* is controlled by the duty cycle of Q1. To improve the efficiency, it's desirable to have Q2 turned ON when Q1 is turned OFF. A simplified switch state diagram is shown in Figure 2 [2]. It depicts the switching sequence as A-B-C-B-A where the state B called "dead time" when both Q1 and Q2 are OFF and the Schottky diode, D1 is ON to provide the freewheeling operation in the inductive load circuit. It's desirable to reduce the dead time to a minimum to improve the efficiency. However, if the dead time is lower than the turn-on or turn-off times of Q1 and Q2, the circuit may go into state D, the shoot-through state when both Q1 and Q2 are ON at the same time causing a short-circuit in the input voltage source, Vin. The state D is undesirable since it would destroy transistors Q1 and Q2.

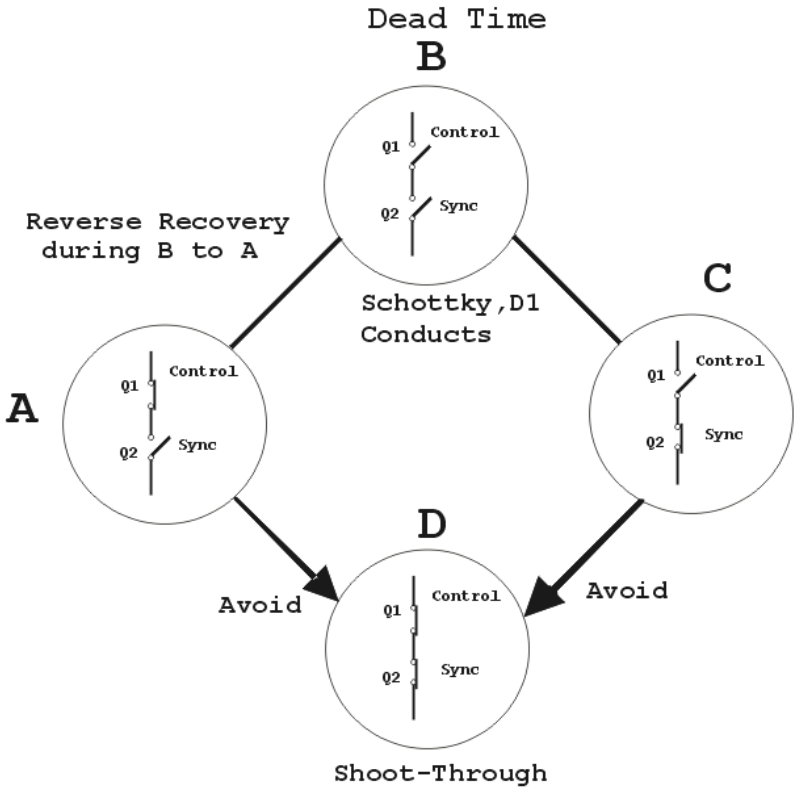

Figure 2: Circuit Switch State Diagram [2]

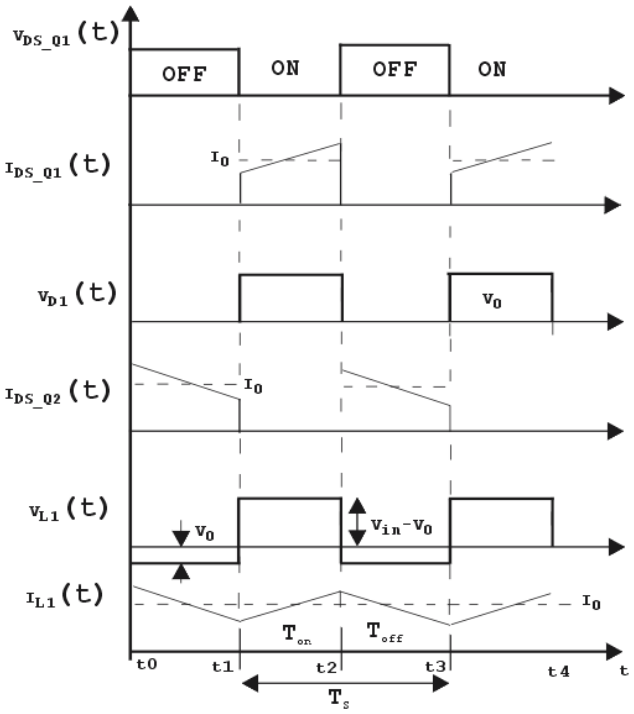

Figure 3: Ideal Circuit waveforms (with no dead time)

The Switching Period, $T_S = T_{on} + T_{off}$, the Switching frequency, $f_S = \frac{1}{T_S}$

The duty cycle, $D = \frac{T_{on}}{T_S} = \frac{T_{on}}{T_{on} + T_{off}}$, Turn-on time, $T_{on} = DT_S$

Turn-off time, $T_{off} = (1-D)T_S$.

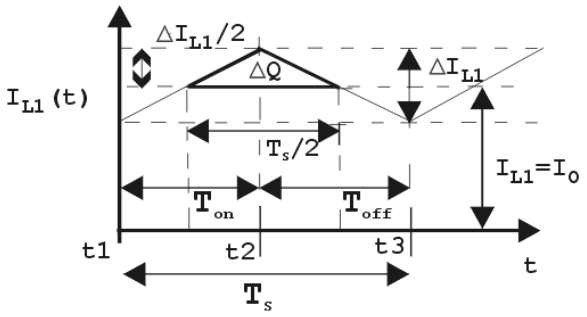

Figure 4: Ideal synchronous buck converter inductor current

An output DC voltage with lowest ripple is considered the best solution. Ripple appears in the output voltage as the L1 current's ripple component, $\Delta I_{L1}(t)$, which charges and discharges the output capacitor, C1, as shown in Figure 4. C1 is charged during the

period when $I_{L1}(t)$ is greater than I_o. The charge (ΔQ) that flows into C1 at this time divided by the value of C1 is the output voltage ripple component.

Output Inductor Ripple Current and Voltage:

The inductor voltage can be defined as,

$V_L = L1\frac{di}{dt} = Vin - Vo$, or, $\Delta i = \Delta I_{L1}(t) = \frac{\Delta t(Vin - Vo)}{L1}$, here, $\Delta t = Ton = DTs$

The inductor ripple current is,

$$\Delta I_{L1}(t) = DTs\frac{Vin - Vo}{L1} = \frac{D(Vin - Vo)}{f_S \bullet L1} \quad (1)$$

The charge, ΔQ, indicated in Figure 5, can be determined by calculating the area of the triangle with height $\frac{\Delta I_{L1}(t)}{2}$ and width $\frac{Ts}{2}$ shown in Figure 5.

$$\Delta Q = \frac{1}{2} \bullet \frac{\Delta I_{L1}(t)}{2} \bullet \frac{T_S}{2} = \frac{\Delta I_{L1}(t) \bullet T_S}{8} = \frac{\Delta I_{L1}(t)}{8 f_S}$$

The ripple voltage is,

$$\Delta V_L(t) = \frac{\Delta Q}{C1} = \frac{\Delta I_{L1}(t)Ts}{8C1} = \frac{D(1-D)VinTs^2}{8L1C1} = \frac{\pi^2(1-D)Vo}{2}(\frac{f_C}{f_S})^2 = \Delta V_O(t) \quad (2)$$

Where, $f_C = \frac{1}{2\pi\sqrt{L1C1}}$, Output low pass filter (LPF) resonant frequency, $f_S =$ The switching frequency. The inductor value of L1 and the effective series resistance (ESR) of the output capacitor, C1, affect the output ripple voltage, ΔV_L. A capacitor with the lowest possible ESR is recommended for the application. For example, 4.7–10 uF capacitors in X5R/X7R technology have ESR approximately 10 mΩ..

Summary of design equations:

Ripples voltage/current, Inductor and Capacitor:

Output ripple voltage, $\Delta V_L(t) = \frac{\Delta I_{L1}(t)Ts}{8C1} = \frac{\Delta I_{L1}(t)}{8C1 f_S}$ (3)

Inductor ripple current, $\Delta I_{L1}(t) = 8C1 f_S \bullet \Delta V_L(t)$ (4)

Output inductor, $L1 \geq DTs\frac{Vin - Vo}{\Delta I_{L1}(t)} = \frac{D(Vin - Vo)}{f_S \bullet \Delta I_{L1}(t)}$ (5)

Output capacitor, $C1 \geq \frac{\Delta I_{L1}}{8 f_s \Delta Vo}$ since $\Delta Q = \frac{1}{2} \bullet \frac{\Delta I_{L1}(t)}{2} \bullet \frac{Ts}{2} = C1 \bullet \Delta Vo$ (6)

Output filter cut-off frequency, $f_C = \frac{1}{2\pi\sqrt{L1C1}}$ (7)

Overview of Synchronous Converter Power Loss: [1]

The losses in the synchronous converter's power switches can be defined by:

$$P_{Total} = P_C + P_{SW} + P_{Gate} + P_{BD} \qquad (8)$$

Where P_C is the conduction loss, P_{sw} is the switching power loss, P_{Gate} is the gate drive loss and P_{BD} is the body diode loss. In addition, inductor equivalent DC resistance losses and output capacitor's ESR loss play significant role in the converter design.

MOSFET Q1 and Q2's Power Loss: [1]

The conduction losses: (replace D to 1-D for Sync FET, Q2):

$$P_C = (I_O\sqrt{D})^2 \bullet R_{DS(on)} \qquad (9)$$

The gate-charge losses:

$$P_{g-C} = V_{GS} \bullet Q_g \bullet f_s \qquad (10)$$

The switching losses:

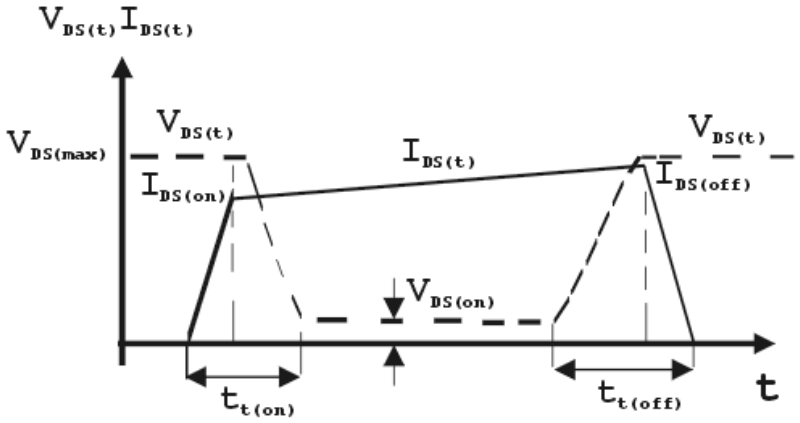

Figure 5: Transitions waveforms of MOSFET for inductive load

The switching loss is,

$$P_{Switching} = P_{t(on)} + P_{t(off)}$$
$$= \frac{[V_{DS(\max)}\{I_{DS(on)} \bullet t_{t(on)} + I_{DS(off)} \bullet t_{t(off)}\} \bullet f_s]}{2} \qquad (11)$$

MOSFET Body Diode Loss: [1]

The body diode loss is a function of dead time and in every switching cycle; there are two dead-time intervals, td1 and td2. The dead-time is defined as the time required when both the MOSFETs Q1 and Q2 are OFF in order to prevent shoot-through.

We can write as:

$$P_{BD} = P_{td1} + P_{td2} \qquad (12)$$

Where Ptd1 is the body diode loss during dead time td1 and Ptd2 is the body diode loss during dead time td2.

$$P_{td1} = P_{cd1} + P_{rr1} = V_f \bullet \left(I_O - \frac{\Delta I_L}{2} \right) \bullet td1 \bullet f_S + \frac{1}{2} \bullet V_{in} \bullet I_{rr} \bullet t_{rr} \bullet f_S \qquad (13)$$

$$P_{td2} = P_{cd2}\left(P_{rr2} = 0\right) = V_f \bullet \left(I_O + \frac{\Delta I_L}{2} \right) \bullet td2 \bullet f_S \qquad (14)$$

PWM Gate Driver Power loss: [1]

The power dissipation in the driver is defined by,

$$P_{DRIVER} = Q_{G(onl)} \bullet V_{DD} \bullet f_S \qquad (15)$$

where $Q_{g(onl)}$ is the total gate charge of the MOSFET and V_{DD} is the driver power supply.

The gate "point of voltage" is,

$$V_{SP} = V_{TH} + \frac{I_O}{g_{fs}} \qquad (16)$$

The driver current is,

$$I_{DRIVER(L-H)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL-UP)} + R_{Gate}} \qquad (17)$$

$$I_{DRIVER(H-L)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL-DOWN)} + R_{Gate}} \qquad (18)$$

The rise time is,

$$t_{t(on)} = \frac{Q_{G(on)}}{I_{DRIVER(L-H)}} \qquad (19)$$

The fall time is,

$$t_{t(off)} = \frac{Q_{G(on)}}{I_{DRIVER(H-L)}} \qquad (20)$$

If an external Schottky diode (D1) is used across Q2, the Schottky's capacitance needs to be charged during Q1 turn-on. The power loss to charge the Schottky's capacitance is,

$$P_{C(SCHOTTKY)} = \frac{C_{SCHOTTKY} \bullet V_{IN}^2 \bullet f_S}{2} \qquad (21)$$

Design Example 1:
Assume design parameters as VIN=12V, VO=3.3V and Io=12A.

Table 1: Design Consideration 1 for synchronous buck converter

Input Voltage, Vin	12V
Output Voltage, Vo	3.3V
Output Current, Io	12A

Assume the output ripple voltage is within $\pm 1\%$ of Vo. For Vo =3.3V, the output ripple is limited within, $\Delta V_L(t) \le 0.033V$. When the output capacitor (C1) is 10uF, the inductor L1 values for the range of switching frequencies from 100 kHz to 500 kHz are given in Table: 2 based on equations 3-7.

Table 2: When C1= 10uF

Vin (V)	Vo (V)	D	ΔV_L (V)	fs (kHz)	C1 (uF)	ΔI_{L1} (A)	L1 (uH)	fc (kHz)
12	3.3	0.275	0.033	100	10	0.264	90	5.31
12	3.3	0.275	0.033	200	10	0.528	45.31	7.48
12	3.3	0.275	0.033	300	10	0.792	30.20	9.16
12	3.3	0.275	0.033	400	10	1.056	22.65	10.60
12	3.3	0.275	0.033	500	10	1.32	18.12	11.83

Synchronous Driver Controller: ISL6594D from Intersil:

Based on equation 18 and 19, From ISL6594D driver datasheet, given high-side: tr=26nS, tf=18nS and source/sink current = 1.25/2A (max). For low-side, trr=18nS, tf=12nS and source/sink current = 2/3.0 A (max):

Table 4: from Datasheet

High-Side	**Rise time**	**Source Current (A)**	**Required Qg(on)**
Source	26 ns	1.25	32.5nC
Sink	18 ns	2	36nC
Low-Side	**Rise time**	**Source Current (A)**	**Required Qg(on)**
Source	18nS	2	36nC
Sink	12ns	3	36nC

ISL6594D Specification:

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LGATE Turn-On Propagation Delay (Note 4)	t_{PDHL}	V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
UGATE Turn-Off Propagation Delay (Note 4)	t_{PDLU}	V_{PVCC} = 12V, 3nF Load	-	10	-	ns
LGATE Turn-Off Propagation Delay (Note 4)	t_{PDLL}	V_{PVCC} = 12V, 3nF Load	-	10	-	ns
LG/UG Three-State Propagation Delay (Note 4)	t_{PDTS}	V_{PVCC} = 12V, 3nF Load	-	10	-	ns
OUTPUT (Note 4)						
Upper Drive Source Current	I_{U_SOURCE}	V_{PVCC} = 12V, 3nF Load	-	1.25	-	A
Upper Drive Source Impedance	R_{U_SOURCE}	150mA Source Current	1.4	2.0	3.0	Ω
Upper Drive Sink Current	I_{U_SINK}	V_{PVCC} = 12V, 3nF Load	-	2	-	A
Upper Drive Sink Impedance	R_{U_SINK}	150mA Sink Current	0.9	1.65	3.0	Ω
Lower Drive Source Current	I_{L_SOURCE}	V_{PVCC} = 12V, 3nF Load	-	2	-	A
Lower Drive Source Impedance	R_{L_SOURCE}	150mA Source Current	0.85	1.3	2.2	Ω
Lower Drive Sink Current	I_{L_SINK}	V_{PVCC} = 12V, 3nF Load	-	3	-	A
Lower Drive Sink Impedance	R_{L_SINK}	150mA Sink Current	0.60	0.94	1.35	Ω

NOTE:

Recommended devices for this application:

1. IXTA90N055T2

VDS = 55V, Id25=90A
Qg(on) = 42nC, Qgs = 14nC, Qgd = 8.5nC,
td(on) = 19nS, tr = 21nS, td(off) = 39nS, tf = 19nS.
Rds(on) = 8.4mΩ
Vgs(th) = 2-4V, g_{fs} = 43
Ciss = 2670pF, Coss = 420pF, Crss = 100pF
Or,

1. **IXTA110N055T2**

Vds = 55V, Id25=110A
Qg(on) = 57nC, Qgs = 16nC, Qgd = 11nC,
td(on) = 18nS, tr = 25nS, td(off) = 40nS, tf = 23nS.
Rds(on) = 6.6mΩ, Vgs(th) = 2-4V, g_{fs} = 49
Ciss = 3060pF, Coss = 497pF, Crss = 105pF

Analysis based on Above IXTA90N055T2:

$$Q_{G(SW)} = 8.5nC + \frac{14nC}{2} = 15.5nC$$

The "point of voltage" is defined by, $V_{SP} = V_{TH} + \frac{I_O}{g_{fs}} = 3 + \frac{15}{43} = 3.35V$

The driver current is,

$$I_{DRIVER(L-H)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL-UP)} + R_{Gate}} = \frac{10 - 3.35}{3 + 2} = \frac{6.65}{5} = 1.33A$$

$$I_{DRIVER(H-L)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL-DOWN)} + R_{Gate}} = \frac{10 - 3.35}{2.2 + 2} = 1.58A$$

The rise time is, $t_{t(on)} = 26nS + 10nS = 36nS$

The fall time is, $t_{t(off)} = 18ns + 10nS = 28nS$

High-Side MOSFET loss (Q1=IXTA90N055T2):

The conduction loss is,

$$P_{Cond\_Q1} = I_O^2 \bullet R_{DS(on)} \bullet D$$
$$= 12^2 \bullet 0.0084 \bullet 0.275 = 0.332 = 332mW$$

The Gate-Charge losses: (assume fs = 200 kHz)

$$P_{GC\_Q1} = V_{GS} \bullet Q_g \bullet f_s = 10.0x42x10^{-9} x200x10^3 = 84mW$$

And estimated switching loss is,

$$\text{Pt} = \frac{[V_{DS(\max)}\{I_{DS(on)} \bullet t_{t(on)} + I_{DS(off)} \bullet t_{t(off)}\} \bullet f_s]}{2}$$
$$= \frac{12 \bullet 12}{2} \bullet (36 + 28)x10^{-9} x200x10^3 = 0.921\text{W}=921\text{mW}$$

Total high-side losses: 332mW+84mW+921mW = 1337mW=1.337W

Low-Side MOSFET loss (Q2):

The conduction loss is,

$$P_{Cond\_Q2} = I_O^2 \bullet R_{DS(on)} \bullet (1 - D)$$
$$= 12^2 \bullet 0.0084 \bullet 0.725 = 0.877W = 877mW$$

The Gate-Charge loss:

$$P_{GC\_Q1} = V_{GS} \bullet Q_g \bullet f_s = 10.0x42x10^{-9} x200x10^3 = 84mW$$

Total low-side losses: 877mW+84mW =961mW

ISL6594D Driver loss:

From datasheet: $V_{DD} = 5V$

Table 6: IXS839 Driver Output Stage from datasheet

Driver pull up resistance	$R_{DRIVER(PULL\_UP)}$	3.0Ω
Driver pull down resistance	$R_{DRIVER(PULL\_DOWN)}$	2.2Ω
Driver gate resistance	R_{GATE}	2Ω

The power dissipation in the driver is defined by,

$$P_{DRIVER} = \frac{T_J - T_a}{R_{thJC}} = Q_{G(total)} \bullet V_{DD} \bullet f_{SW}$$

where V_{DD} = 10V and f_S = 200 kHz (assume for this case)

The estimated driver power dissipation, $P_D \approx 42 \bullet 10^{-9} \bullet 10 \bullet 200 \bullet 10^3 = 84mW$

Dead-Time Power Loss: [3]

The dead-time is defined as the time required when both the MOSFETs are off in order to prevent shoot-through. In this period, the Schottky diode (or integral body diode is forward-biased and provided a power loss defined by,

Driver IXS839 provides delay time in the datasheet,

$$t_{Delay\_Time}(nS) = C_{Delay}(pF) \bullet (0.5nS / pF) \qquad (22)$$

Assume, $t_{d1} = t_{d2} = 100nS$, which provides $C_{Delay}(pF) = 200pF$

The Delay-Time loss is define in (11-13) as

$$P_{td1} = P_{cd1} + P_{rr1} = V_f \bullet \left(I_O - \frac{\Delta I_L}{2} \right) \bullet td1 \bullet f_S + \frac{1}{2} \bullet V_{in} \bullet I_{rr} \bullet t_{rr} \bullet f_S$$

$$= 0.85 \bullet \left(12 - \frac{0.528}{2} \right) \bullet 100x10^{-9} \bullet 200x10^3 + \frac{1}{2} \bullet 12 \bullet 2.2 \bullet 37x10^{-9} \bullet 200x10^3$$

= 0.19905+0.09768= 0.297W= 297mW

$$P_{td2} = P_{cd2}(P_{rr2} = 0) = V_f \bullet \left(I_O + \frac{\Delta I_L}{2} \right) \bullet td2 \bullet f_S$$

$$= 0.85 \bullet \left(12 + \frac{0.528}{2} \right) \bullet 100x10^{-9} \bullet 200x10^3 = 0.208W = 208mW$$

$$P_{BD} = P_{td1} + P_{td2} = 297mW + 208mW = 505mW$$

Synchronous Converter Efficiency:

If we neglect inductor's DC power loss and capacitor's ESR loss then the total estimated power loss, P_{loss}= 1337mW+1007mW+84mW+505mW=2933mW= 2.933W

Given output power, Po = Vo*Io = 3.3*12= 39.6W

Estimated input power, Pin= 39.6+2.933=42.6W

The efficiency is defined as, $\eta = \frac{VoIo}{Vin \bullet Iin} = \frac{Po}{Pin}$ (23)

The estimated efficiency, $\eta = \frac{39.6}{42.6} = 0.93 = 93\%\,\%$,

Estimated input current:

If we assume only 93% efficiency, then the estimated input current can be obtained,

Estimated input current, $I_{in} = \frac{VoIo}{Vin \bullet \eta} = \frac{3.3 \bullet 12}{12 \bullet 0.93} = 3.5A\,\mathrm{A}$

Bootstrap Circuit Design: [3]

Selecting bootstrap circuit components are done with consideration of the electrical rating and characteristics of the high-side MOSFET (Q1).

The capacitance is defined by datasheet of IXS839 driver,

$$C_{BST} = \frac{Q_{G(total)}}{\Delta V_{BST}} \qquad (24)$$

Where $Q_{G(total)}$ is the total gate charge of high-side MOSFET (Q_1), and $\Delta VBST$ is the allowable voltage droop in Q_1. Assume this voltage droop equal to 0.1V.

$$C_{BST} = \frac{42nC}{200mV} = 0.210uF$$

The bootstrap diode and capacitor voltage rating should be

$$V_{Bootstrap\_DiodeandCapacitor} > V_{IN} + V_{DD}$$

The average forward current is defined by,

$$I_{F(Avg)} = Q_{G(total)} \bullet f_{SW} \qquad (25)$$
$$= 42 \bullet 10^{-9} \bullet 250 \bullet 10^{3} = 10.5mA$$

Bibliography

[1] “Synchronous Buck MOSFETs loss calculation” AN-6005, Jon Klein, Fairchild Semiconductor, 01/04/2006, www.fairchildsemi.com

[2] “Examination of reverse recovery losses in a synchronous buck converter circuit” Application Note from Silicon Semiconductor, 2003, www.siliconsemi.com

[3] Datasheet for ISL6594D “Advanced Synchronous Rectified Buck MOSFET Driver” from Intersil Corporation, 2007, www.intersil.com